Advanced Packaging for Heterogeneous Integration

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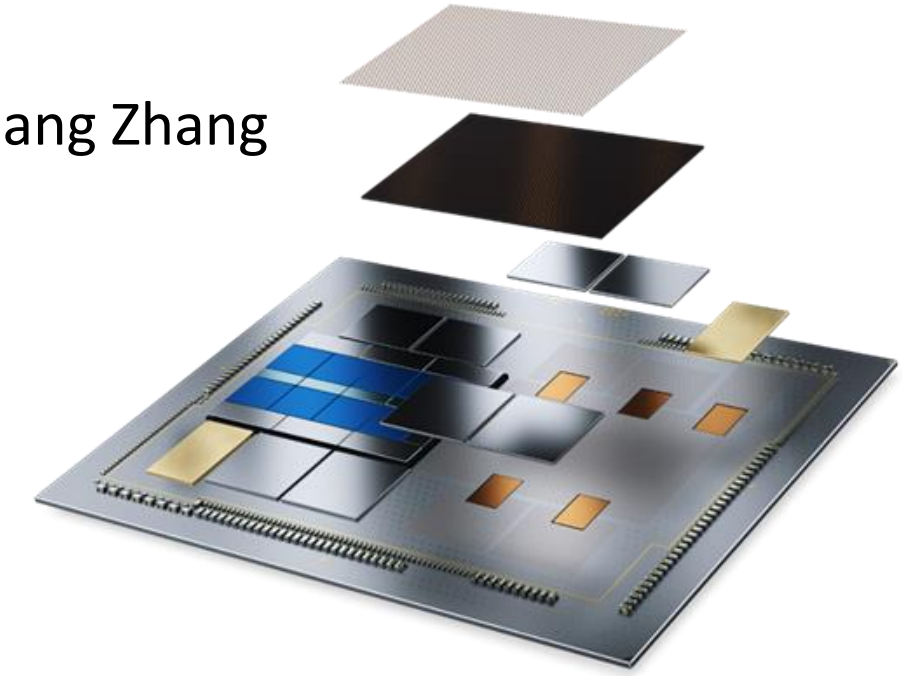
November 2021



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Executive Summary

- Heterogeneous Integration (HI) is an important vehicle to drive continued advances in Micro-electronics
- Advanced Packaging Architectures today provide unprecedented levels of Heterogeneous Integration in Client, Server and Discrete Graphics
- The vision is to develop heterogeneously integrated leadership products using advanced packaging technologies to match the functionality of a monolithic SOC (and more)
- Future products face a slew of complex performance and manufacturing demands along multiple vectors
- We as a community must collaboratively extend advanced packaging technology envelopes along multiple vectors to meet the demands of the future

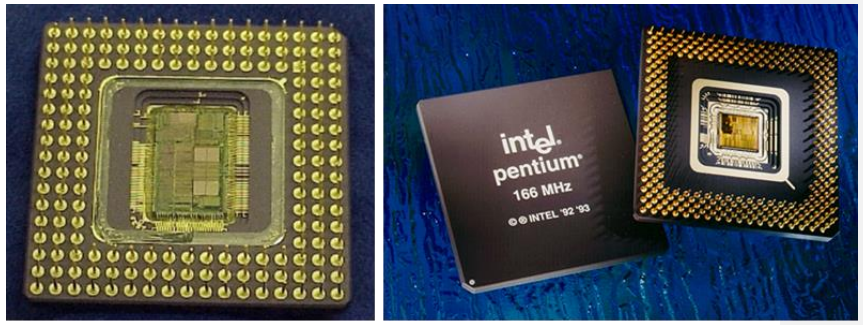
Historical Context

“Quiet” Revolutions in Packaging

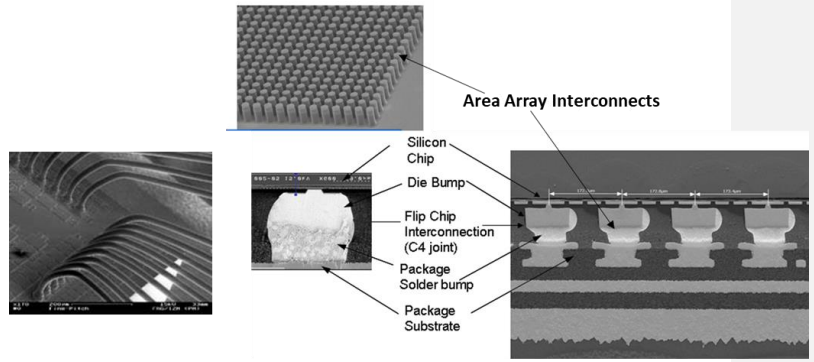
1990s : Packaging revolutionized by launch of the **first flip-chip organic substrate**; A New Package Industry is born

2000s : Copper Pillar Bumps on die are introduced as an extension on Cu backend; Intel leads the industry by deploying **fully lead & halogen free packages**; High Pin Count Land Grid Sockets Become Mainstream; Drive to greater adoption of Ball Grid Arrays enables “Small and Thin”

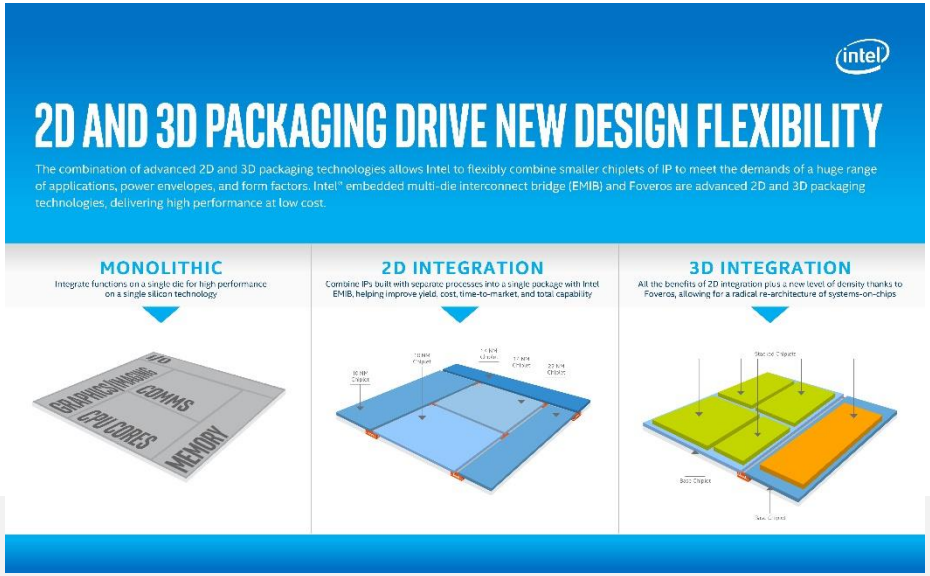
2010s : Thermo-Compression Bonding Tools enable Fine Pitch Flip-Chip; **Multiple Breakthrough 2D Multi-Chip Packaging Technologies (CoWOS, EMIB, FOCOS)** Introduced : **HBM, Foveros, SOIC open up the 3rd Dimension**



Ceramic Packaging → Organic Packaging



Wire-Bond → Organic Flip-Chip



Thermo-compression Bonding for Fine-pitch Copper-pillar Flip-chip Interconnect – Tool Features as Enablers of Unique Technology

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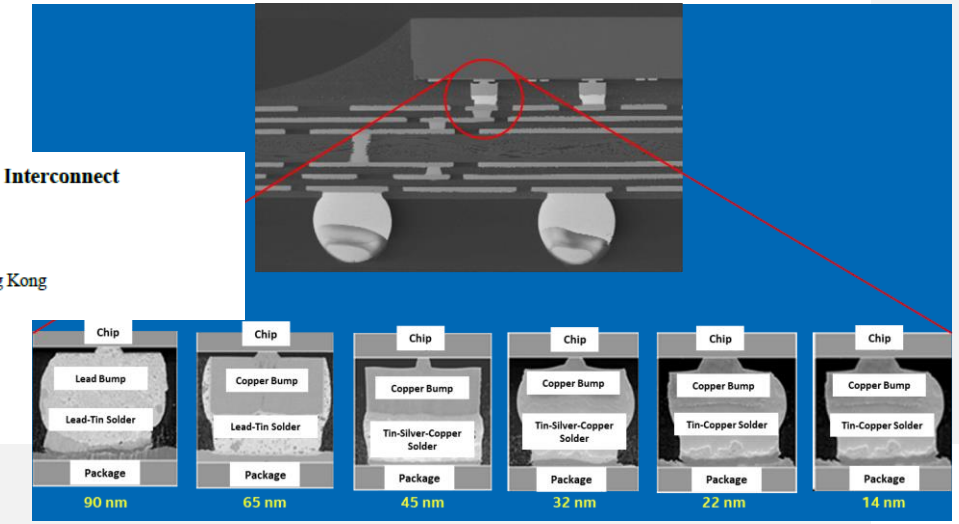
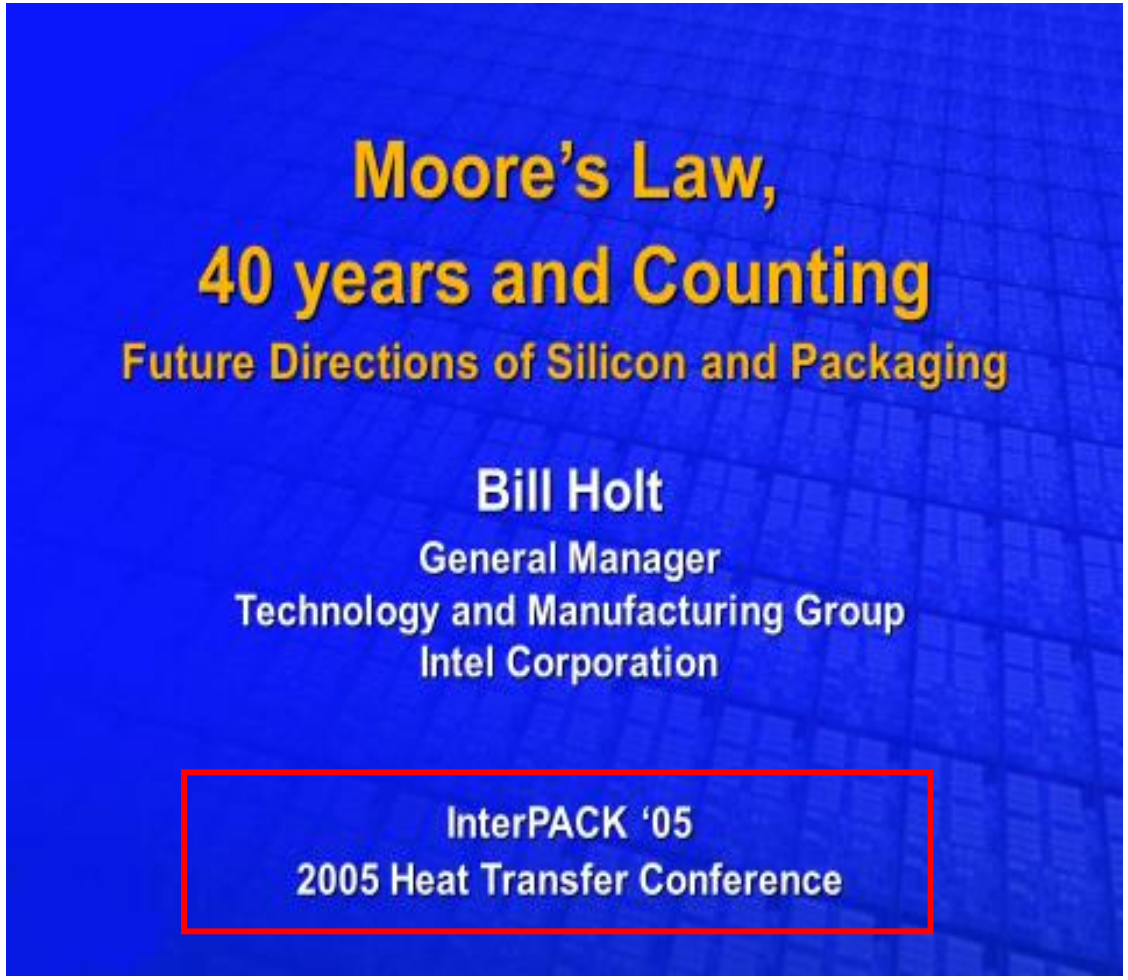


Packaging Today

Packaging for HI is Not a New Idea*



***Heterogeneous Integration is the integration of separately manufactured & tested components into a higher level assembly (SiP aka MCP) that, in the aggregate, provides enhanced functionality and improved operating characteristics (Ack: Bill Chen, Bill Bottoms)**

And it is part of a broad Industry wide Roadmap

Heterogeneous Integration Roadmap (HIR)

Launched 10-10-2019
24 chapters
590 Pages
Free download
Download Link
https://eps.ieee.org/technology/heterogeneous-integration-roadmap

- Sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division
- Comprehensively covering microelectronics technology ecosystem
- Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions
- HIR is the Knowledge Roadmap & Knowledge Supply Chain for the Heterogeneous Future

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Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Cross Cutting Technologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (new chapter for 2021)

Heterogeneous Integration Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communications & Beyond

Integration Processes

- SiP
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Co-Design & Simulation

- Co-Design & Simulation – Tools & Practice

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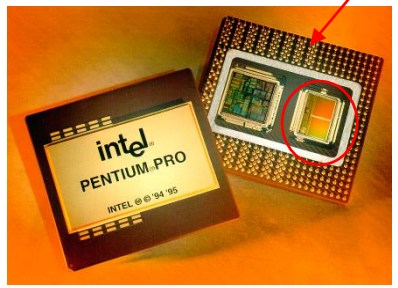
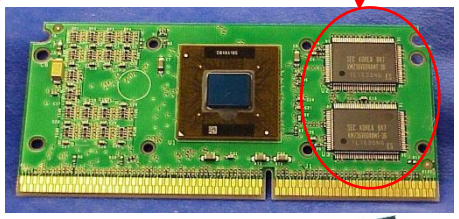
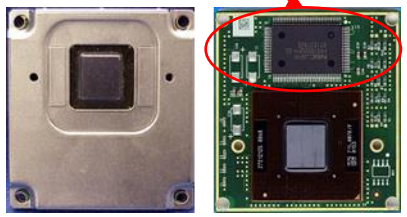
Intel has a long history of using MCPs for Time to Market (TTM) & Performance….

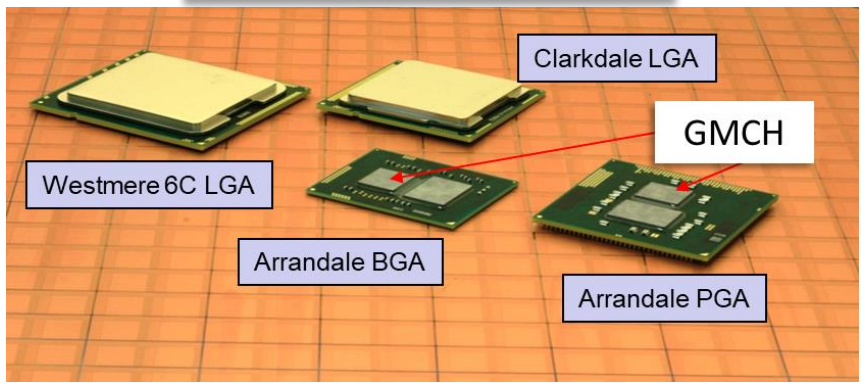
SRAM Integration

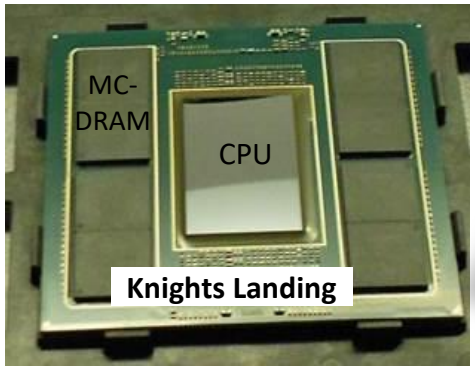


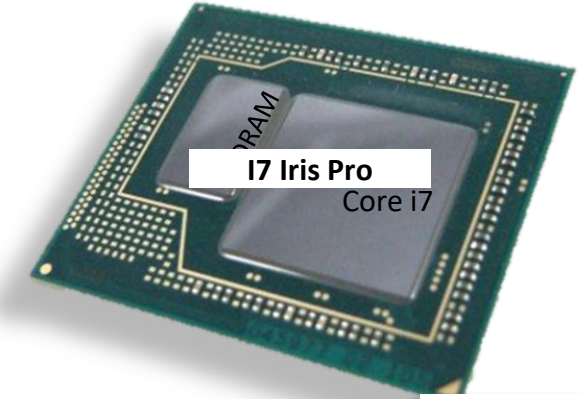


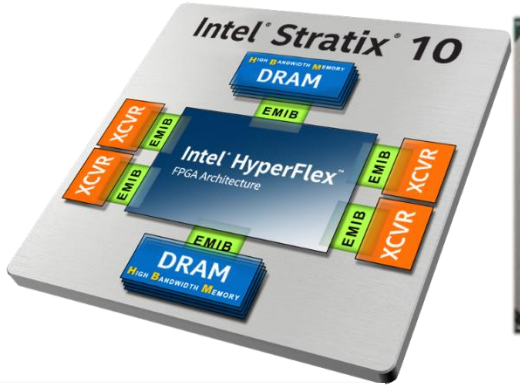


(G)MCH Integration





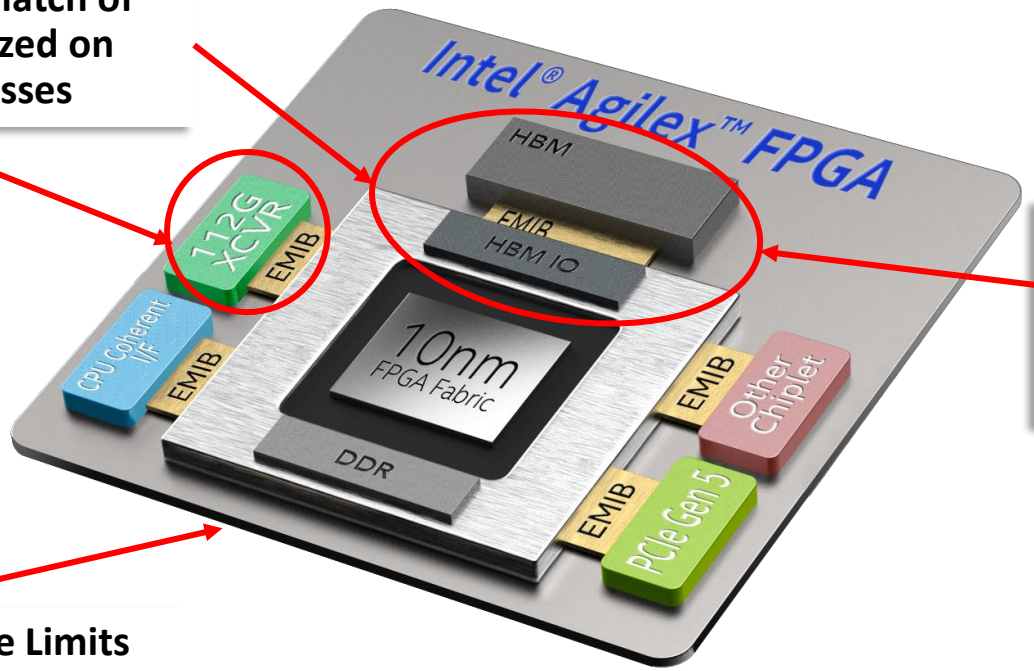




DRAM Integration

Increased Interest in HI is Driven by ..

Need to Mix and Match of Diverse IP Optimized on Different processes

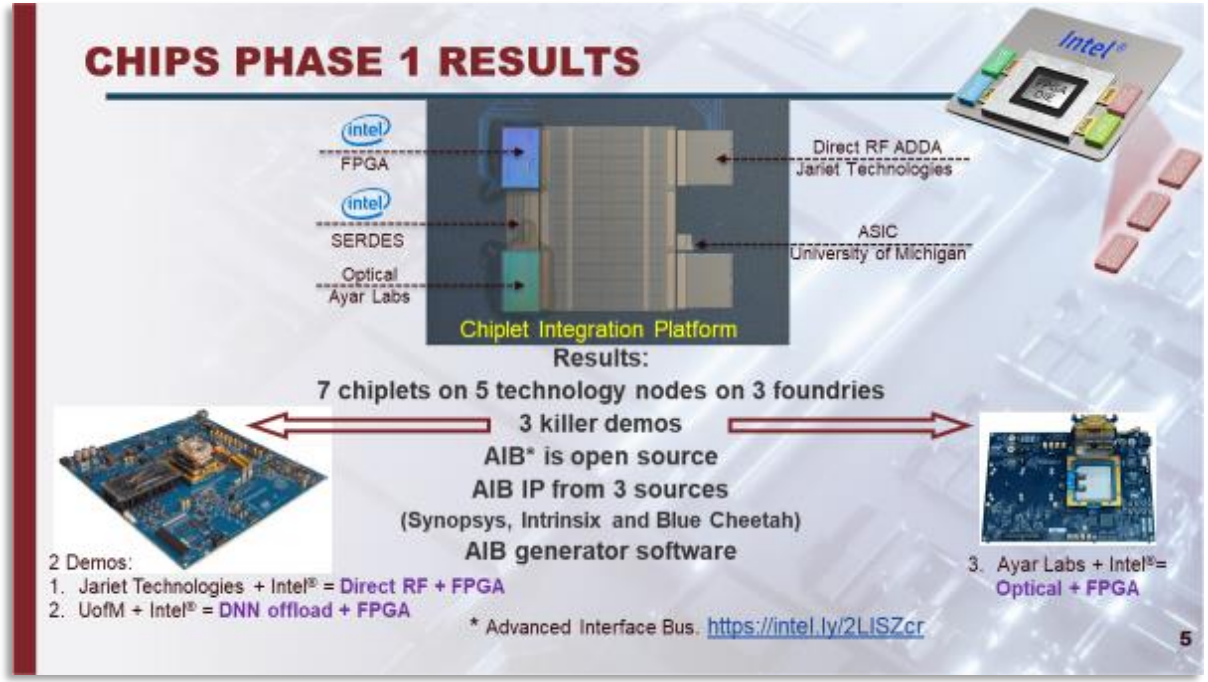


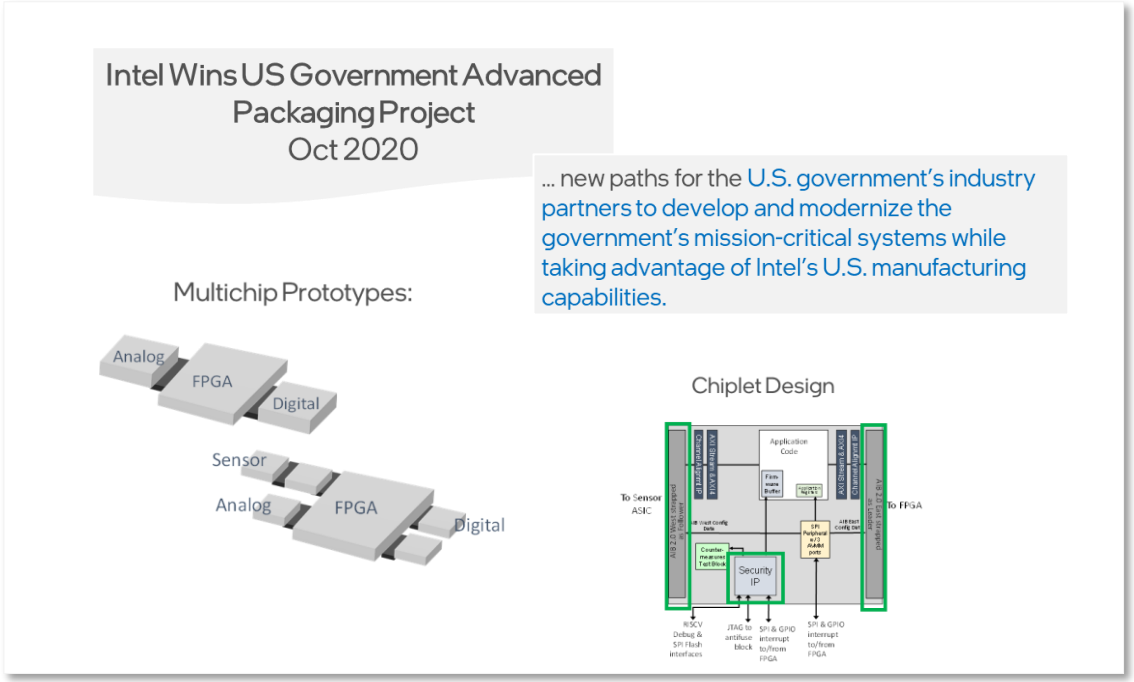
Need for Proximate Memory with a High BW Low Power Interface

Escape from Reticle Limits

Additionally, Yield Resiliency and TTM Advantages Make On-Package HI Attractive

The Package is a Compact HI Platform For Several Interesting Use Cases

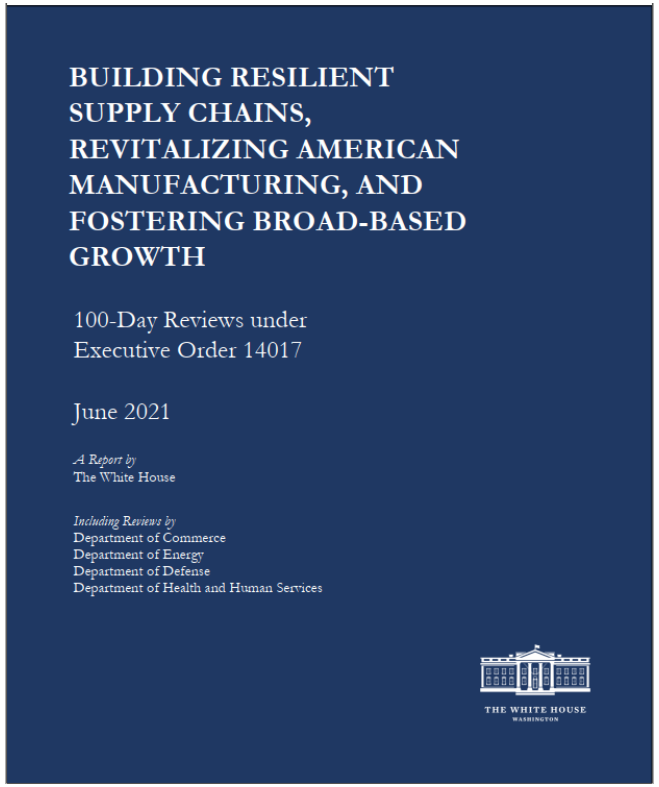




HI expands possibilities of on-package functionality : Standardized Interfaces help

Sources: Intel Architecture Day (2021) & ERI Summit (2020). The CHIPS work is supported by the DARPA MTO office (DARPA CHIPS Program))

Advanced Packaging Offers a Critical Strategic Advantage

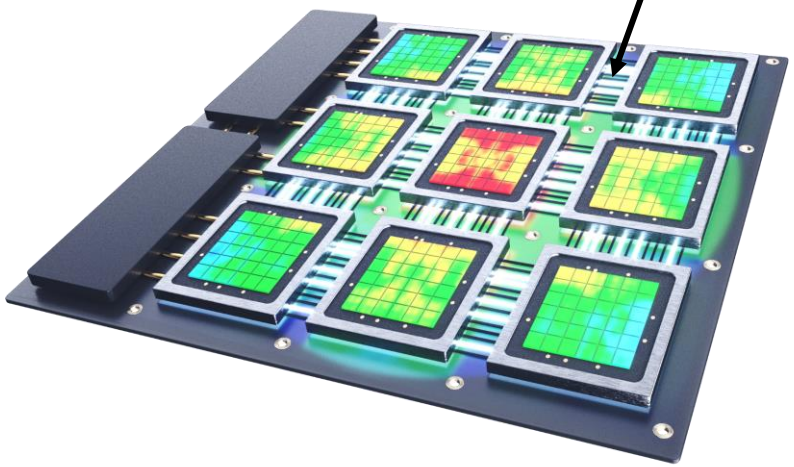


Semiconductor manufacturing and advanced packaging: Semiconductors are an essential component of electronic devices. The packaging, which may contain one or more semiconductors, provides an alternative avenue for innovation in density and size of products. Semiconductors have become ubiquitous in today's world. They enable telecommunications and grid infrastructure, run critical business and government systems, and are prevalent across a vast array of products from fridges to fighter jets. A new car, for example, may require more than 100 semiconductors for touch screens, engine controls, driver assistance cameras, and other

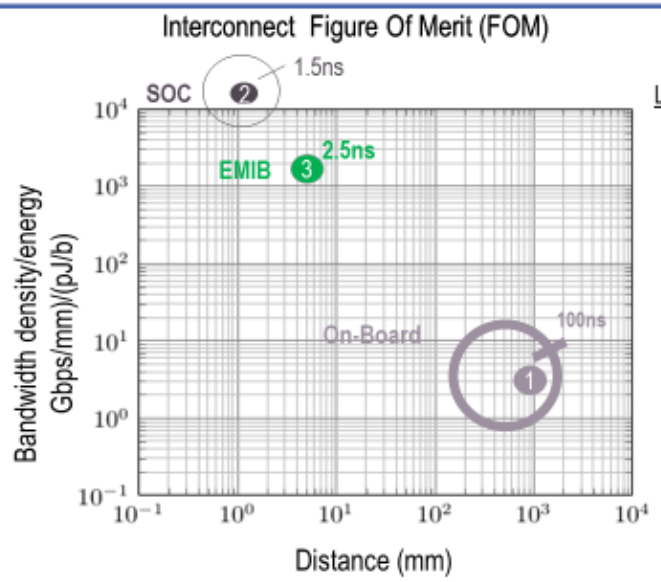
"BUILDING RESILIENT SUPPLY CHAINS, REVITALIZING AMERICAN MANUFACTURING, AND FOSTERING BROAD-BASED GROWTH", A report by the White House, June 2021.

Packaging Vision - Raja Koduri (2018)

Develop and own leadership technology to connect chips and chiplets in a package to match the functionality of a monolithic SOC



EMIB = SoC Like FOM



Legend:
##ns Solution latency
Solution space

1. On-Board interconnect (e.g. PCI-E PMA + PCS):
   - ~1000mm; ~0.3mm shoreline; 20pJ/bit; 16Gbps:
   - FOM=(16Gbps/0.3mm)/(20pJ/bit)=2.7
   - Latency=100ns

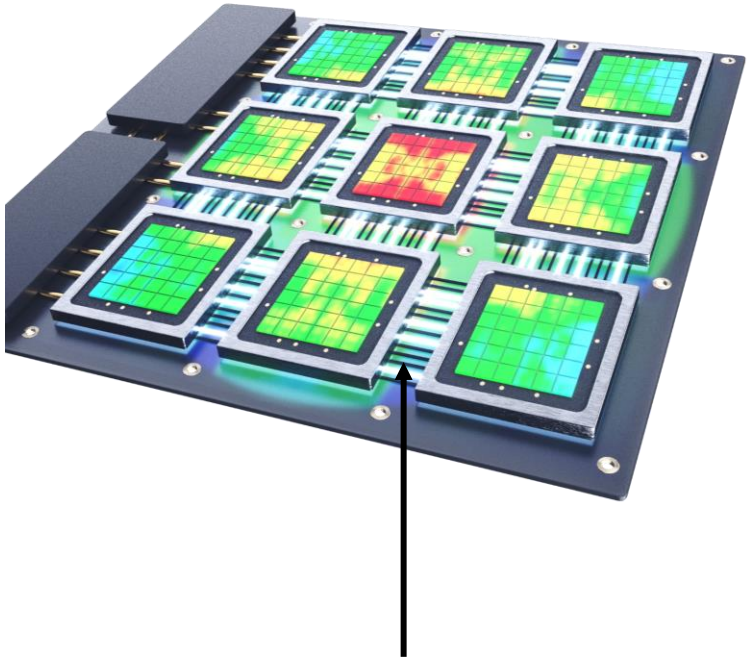
3. EMIB based (55um ubumps)
   - FoM = (1Tbps/mm)/(0.85pJ/bit) = 1,250
   - Latency=2.5ns

2. SOC (12invs+2DFF+2mux):
   - ~1mm; ~1um shoreline; 0.1pJ/bit; 2Ghz:
   - FOM=(2Gbps/0.001mm)/(0.1pJ/bit)=20,000!
   - Latency=1.5ns

Breakthrough Packaging Technologies Approach SOC-like Connectivity Capabilities

High density interconnect that enables high bandwidth @ low power is essential to realize this vision

Interconnects in Advanced Packaging….



2D Interconnect

3D Interconnect

DARPA The Serial vs. Parallel Question

Source: Presentation by Andreas Olofsson @ DARPA 2.5D/3D Workshop, Dec 6, 2018

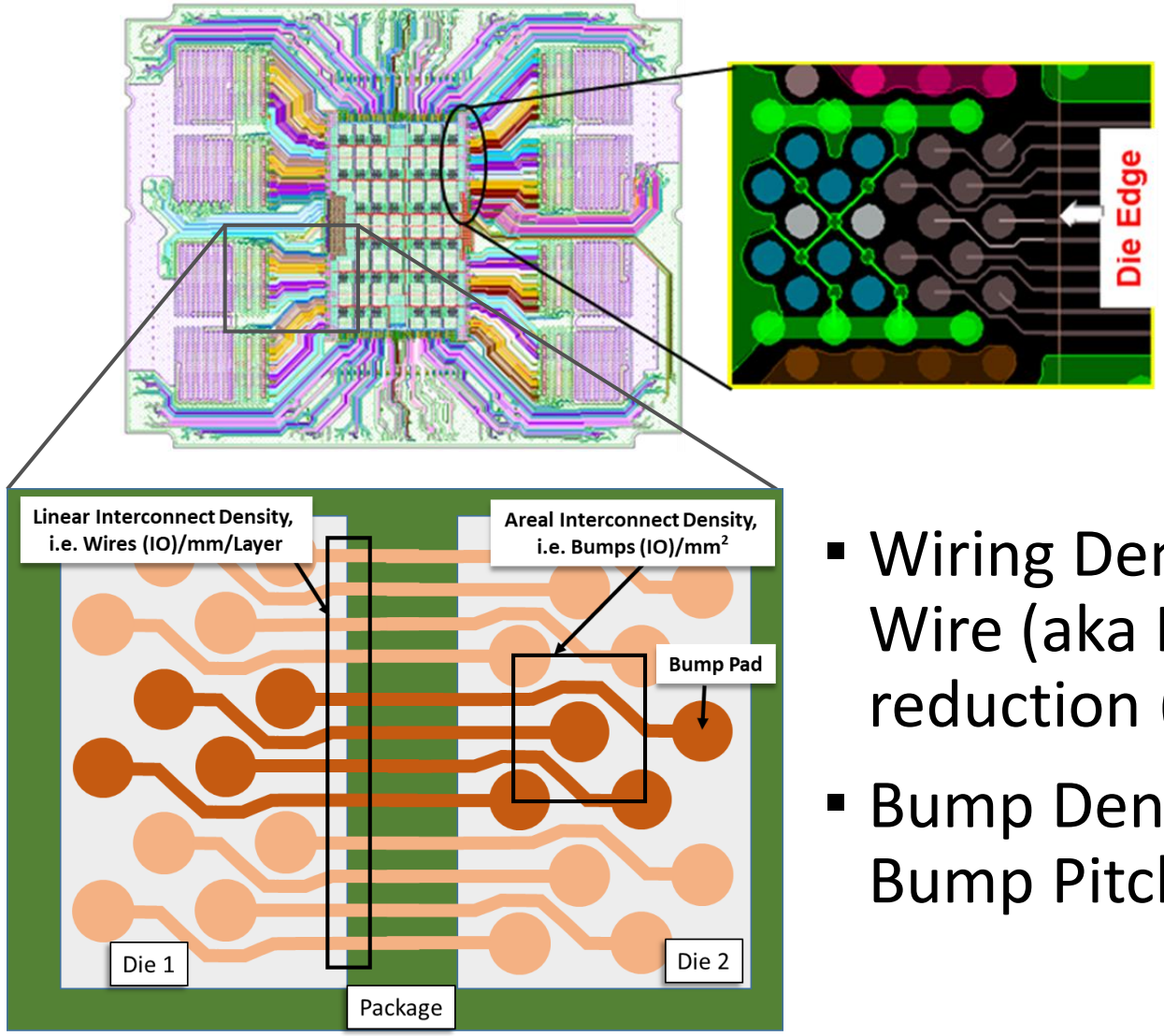
	CHIPS Parallel		Serial
IP Complexity	Flip-flop + tristate		SERDES
IP Cost	Low		High (open source?)
Throughput	1Tbps/mm		1Tbps/mm?
Latency	<5ns		High
Energy Efficiency (<1000um)	0.1pJ/bit	Physics	1-10pJ/bit
Throughput per pin	2Gbps		30Gbps
Packaging Complexity	High		Low
Packaging Cost	High	Economics?	Low

Parallel will continue to be the chosen path for DARPA until someone makes a valid case for a different option.

Distribution Statement "A" (Approved for Public Release, Distribution Unlimited) 11

High Bandwidth, Low Power, Parallel Links drive Need for High Density Die-Die Interconnects

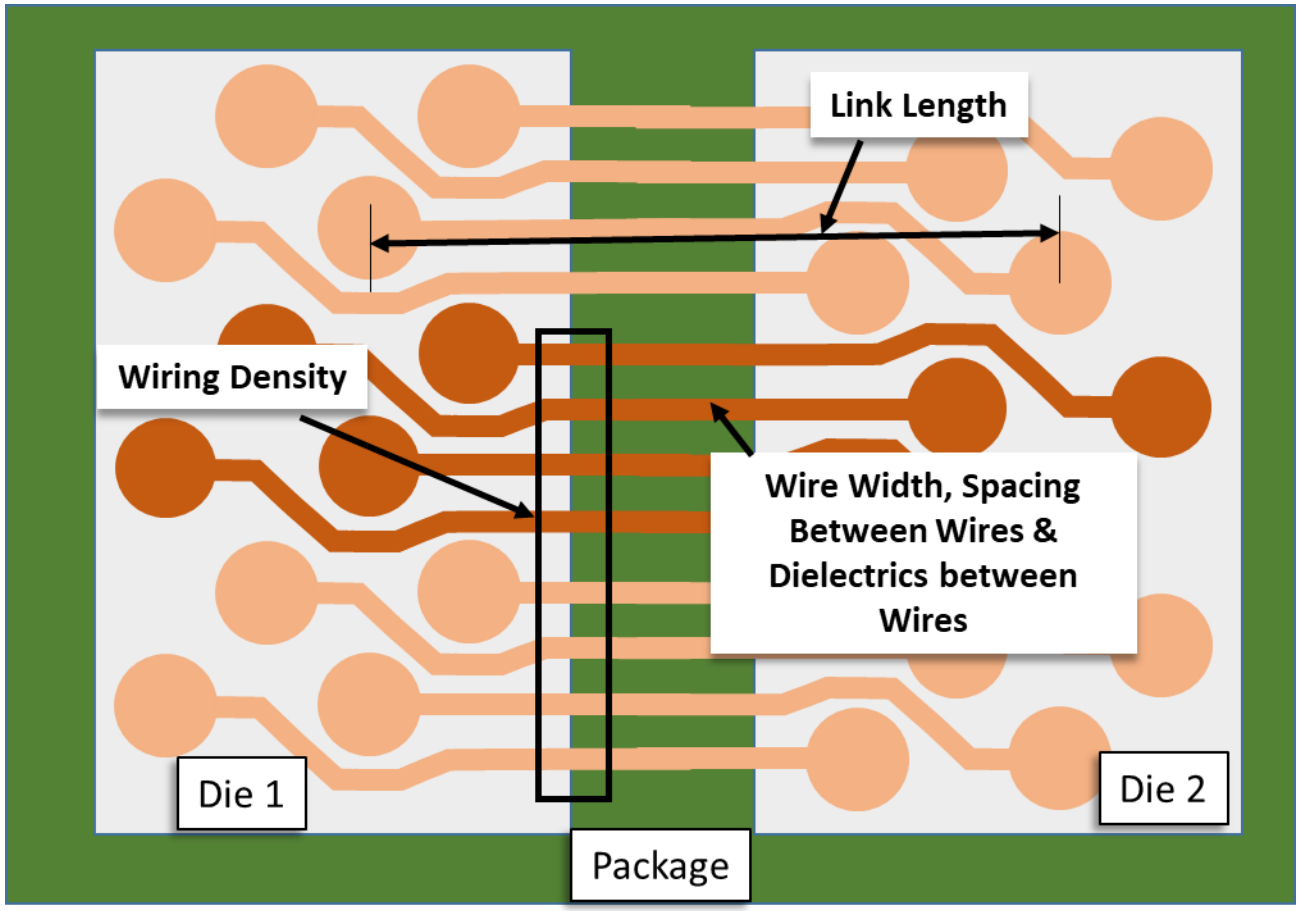
Physical Metrics for High Density Interconnects



- Wiring Density increases Require Wire (aka IO) Width, Space & Pad reduction (Zero Pad Ideal)
- Bump Density Increases Require Bump Pitch Shrinks

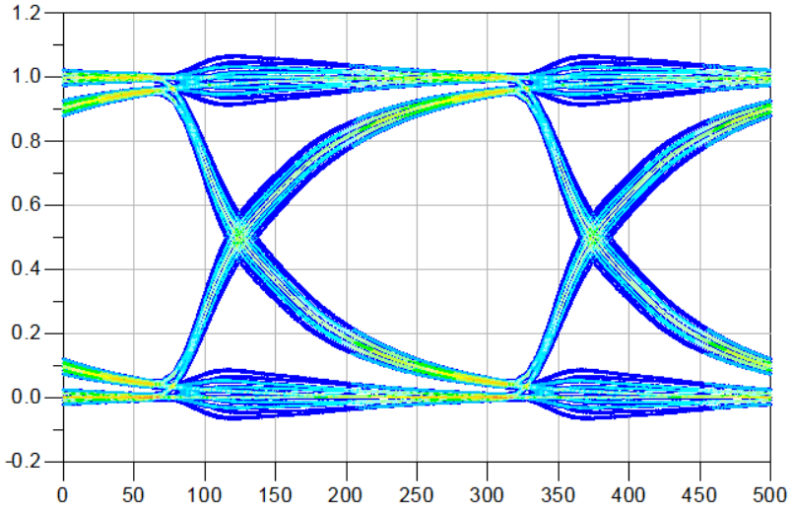
Signaling Considerations in High Density Interconnects

Key factors Affecting Signal Integrity and Power efficiency

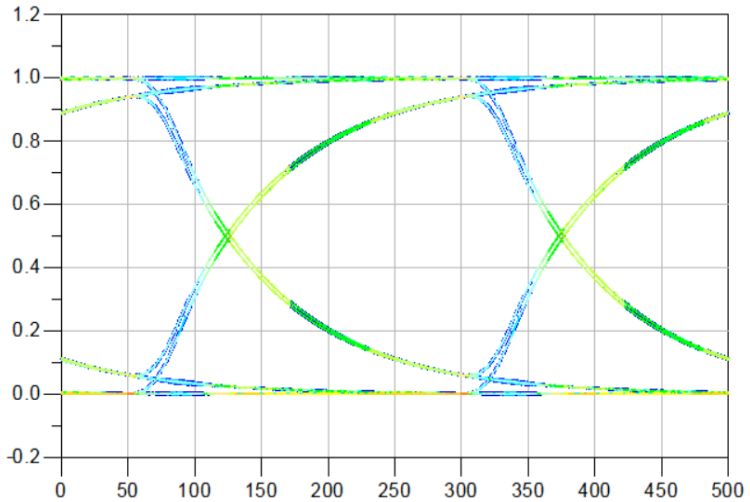


Signaling Considerations in High Density Interconnects

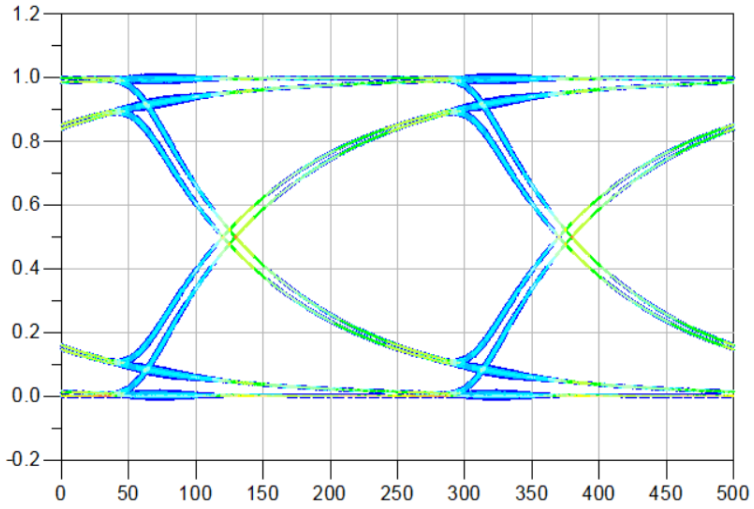
3S:1G 500 Wires/mm

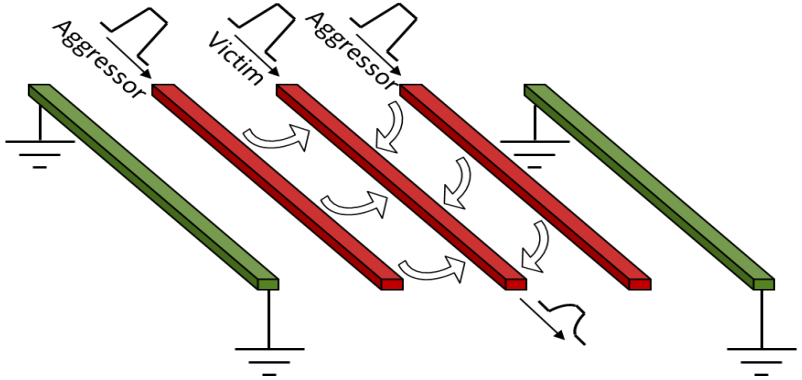


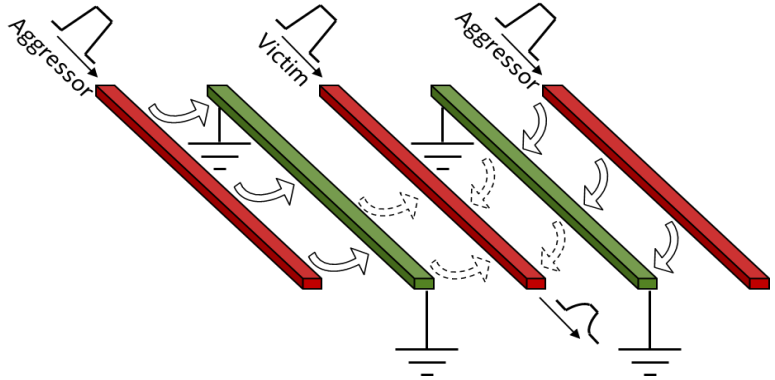
1S:1G 500 Wires/mm



1S:1G 1000 Wires/mm



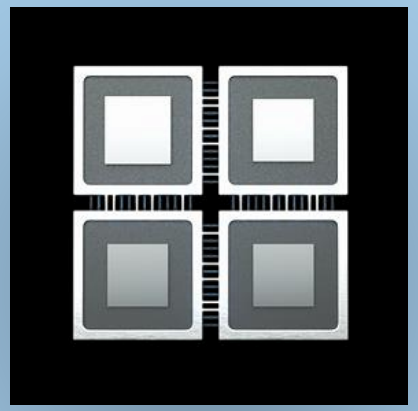


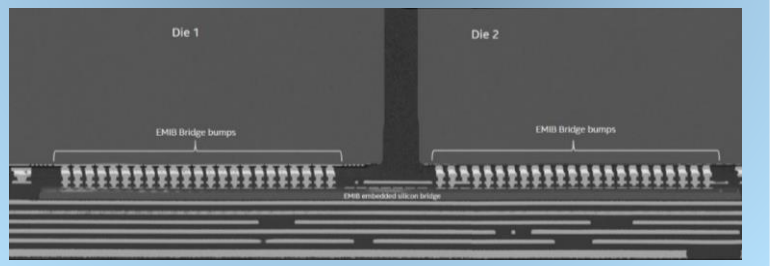


1. **For Details on Optimization See A.C. Durgun, et. al. "Electrical performance limits of fine-pitch interconnects for heterogeneous integration," IEEE ECTC, Las Vegas, NV, 2019**
2. **Simulations above assume a link length of 0.8mm**

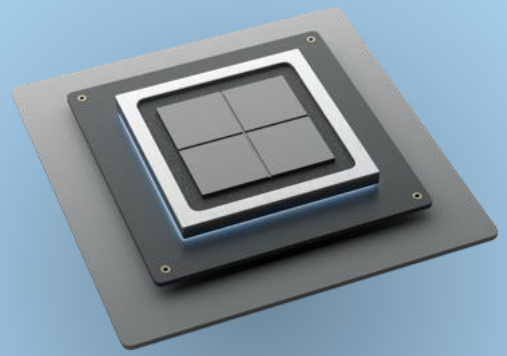
Current State of Advanced Packaging (Intel Centric View)

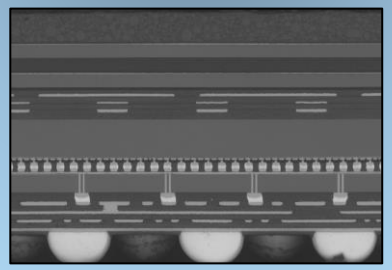
EMIB



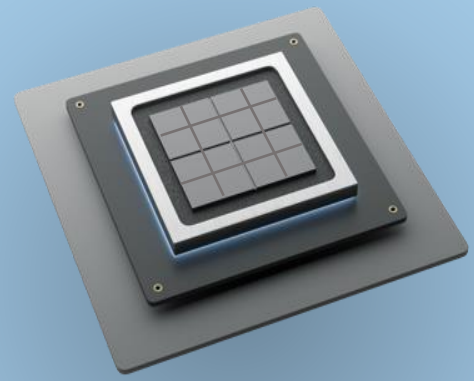


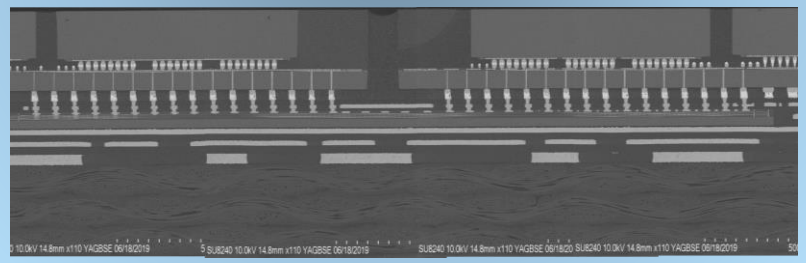
Foveros





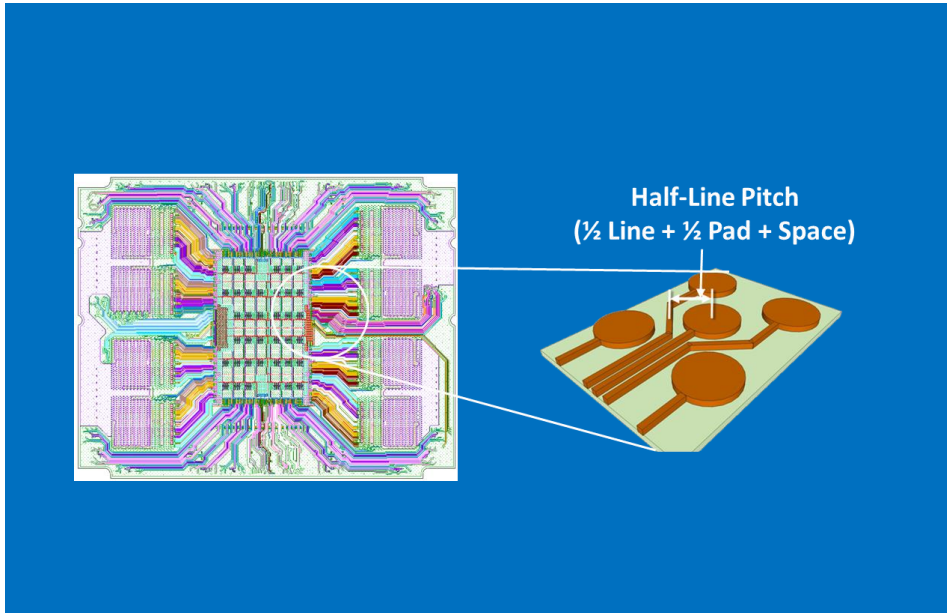
EMIB-Foveros

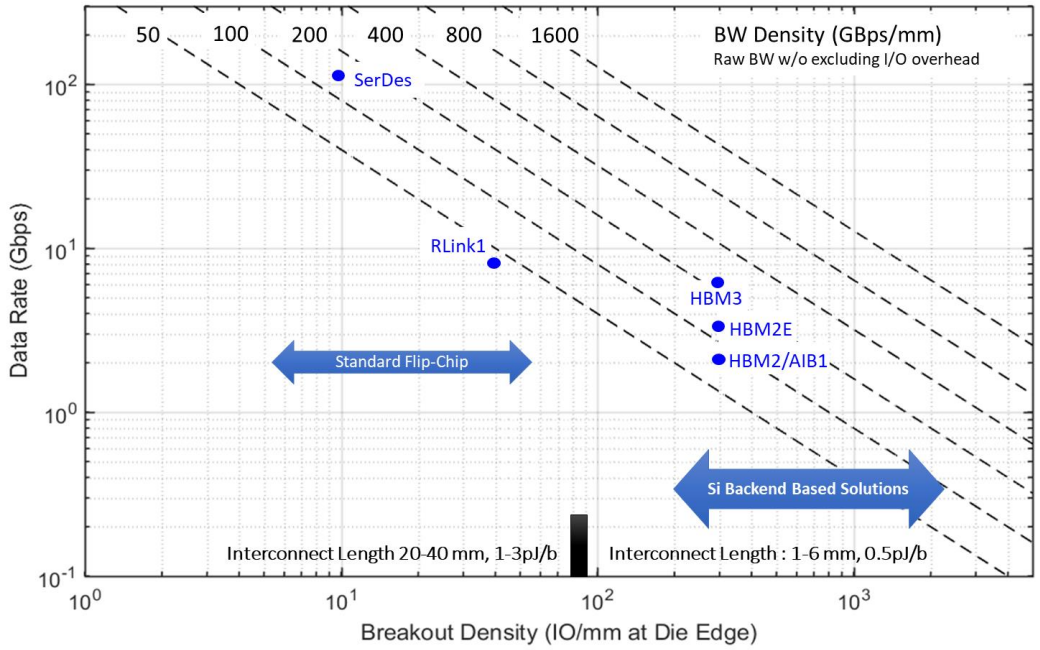


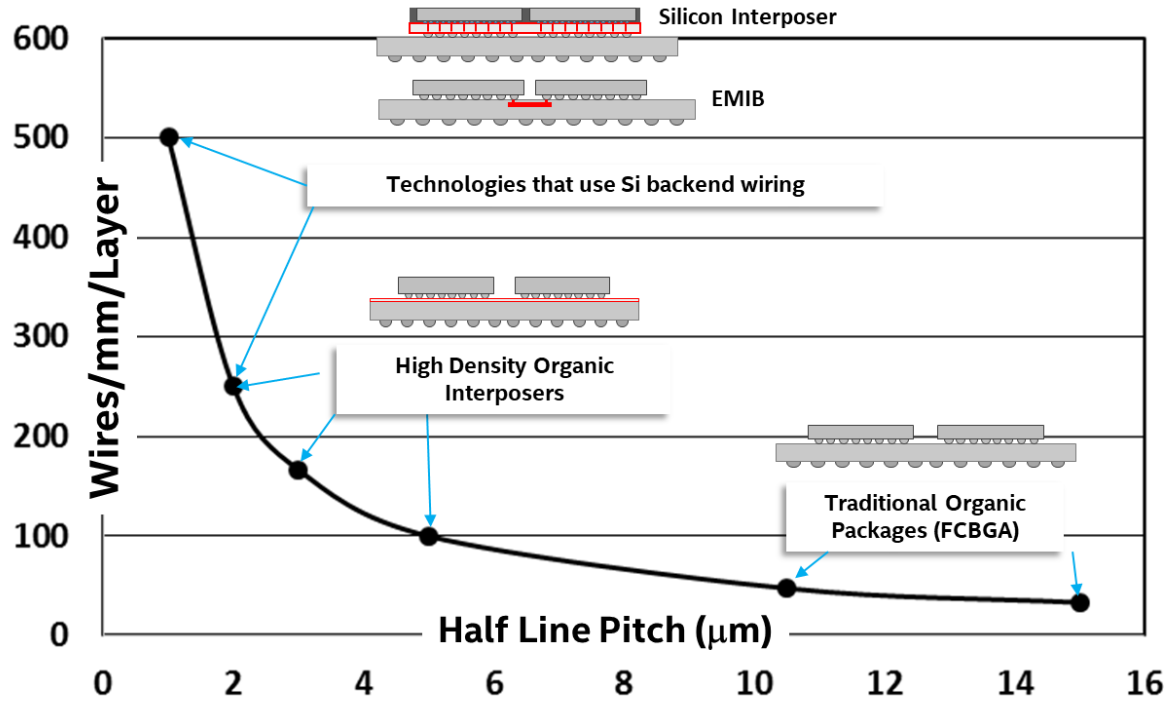


Several Advanced Packaging Architectures available today for Scaling in all 3 directions : They have opened Product Arch Opportunities that didn't exist just a decade ago!

Planar Interconnects - MCP Landscape



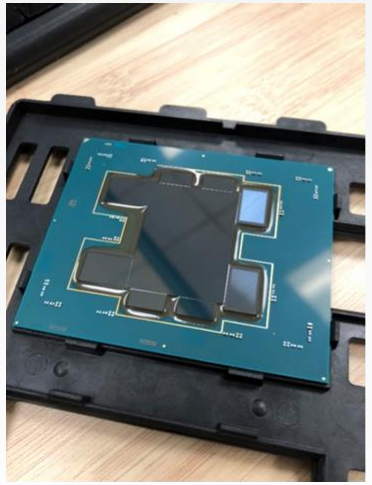


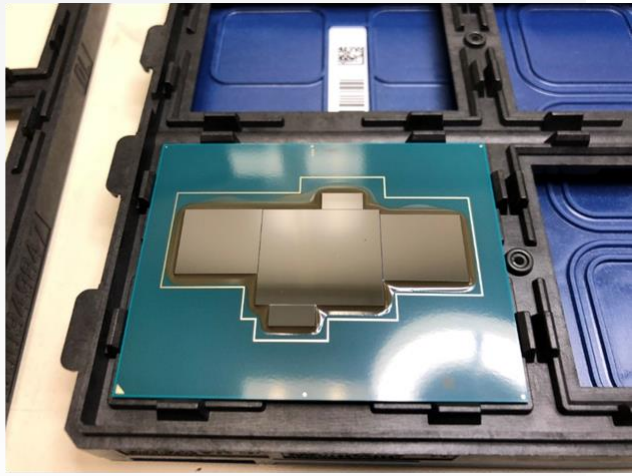


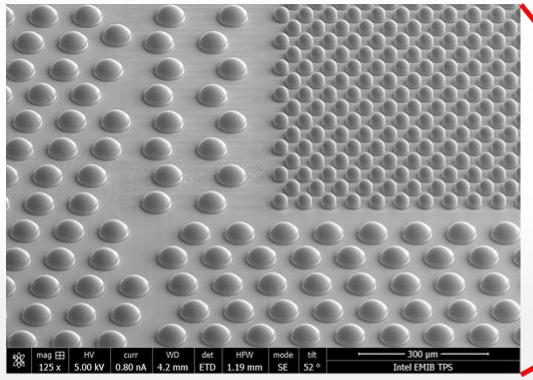
Our Focus : Push Interconnect Density for Increased BW + Improved Power Efficiency

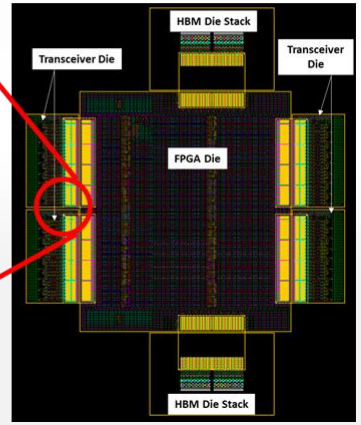
EMIB Embedded **M**ulti-Die **I**nterconnect **B**ridge

- Localized high-density wiring
- Multiple Bridges, Multiple Bridge Sizes and Bridge Technologies
- Bridge Mix and Match → Enhanced Design Flexibility
- Bridge silicon costs < Silicon interposer
  - No TSVs, Significantly less silicon area
- Die from Different Foundries
- Large Overall Die Area enabled



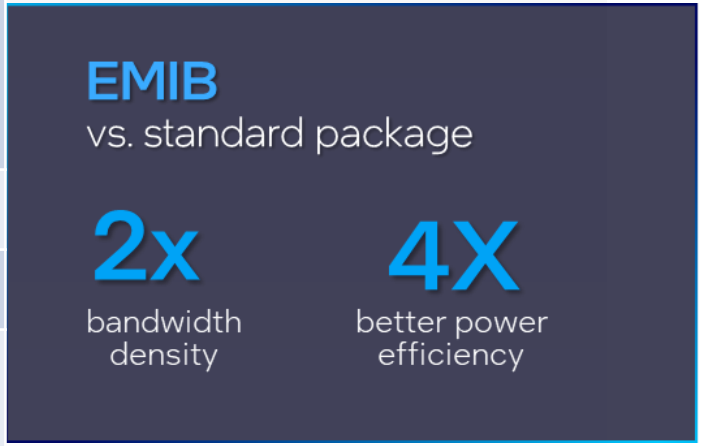






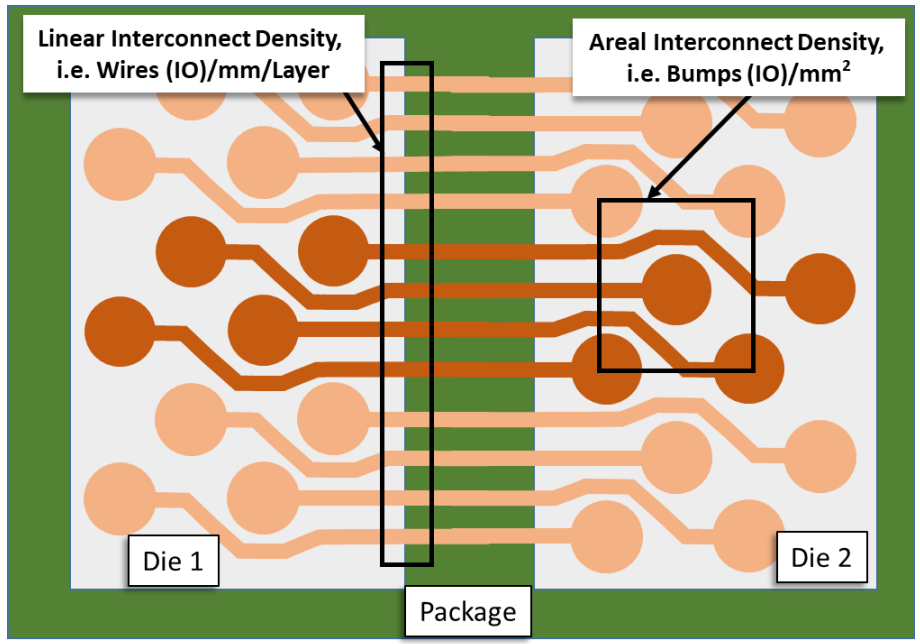
EMIB Link Capability

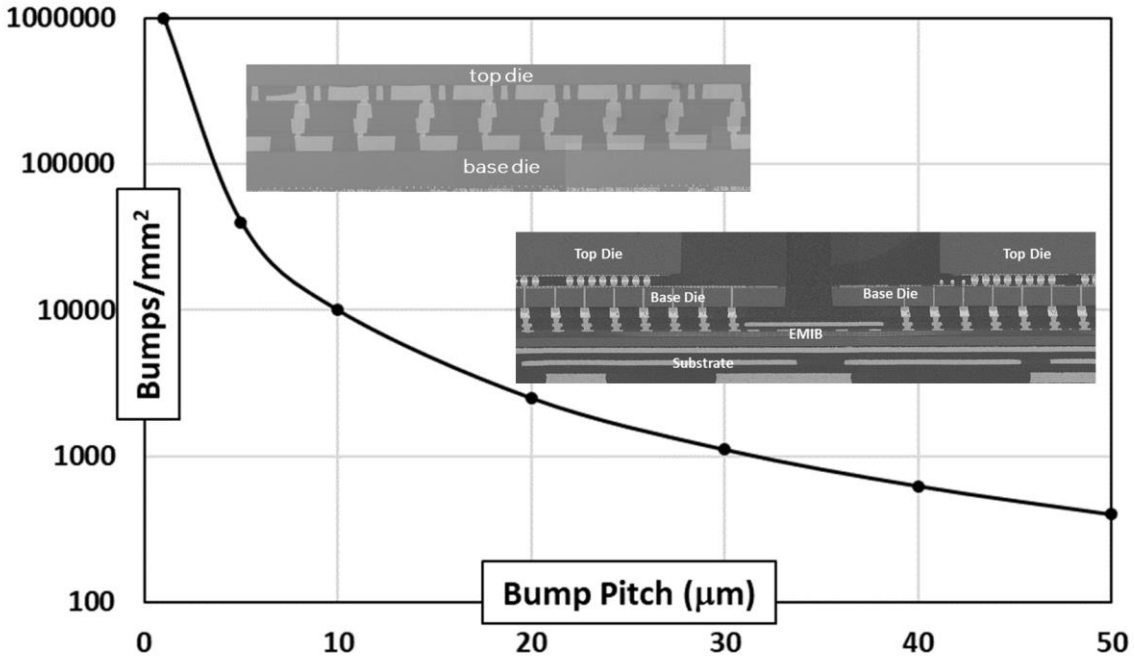
	Intel MDF	Intel OPIO	Improvement due to EMIB
Packaging Tech	EMIB	Standard 2 routing layers	
Bump Pitch (µm)	55	110	
Pin Speed (Gbps)	5.4	8 – 16	
Shoreline BW density (GBps/mm)	196	34.5 – 69	5.68x – 2.84x
Areal BW density (GBps/mm²)	158	36.7 – 73.4	4.3x – 2.15x
PHY power efficiency	0.5	1.5-2.0	3x – 4x



- Intel MDF was announced in Semicon West 2019.
- Intel OPIO 8Gbps was used in a Client in 2013. Higher speeds were developed in an internal study.

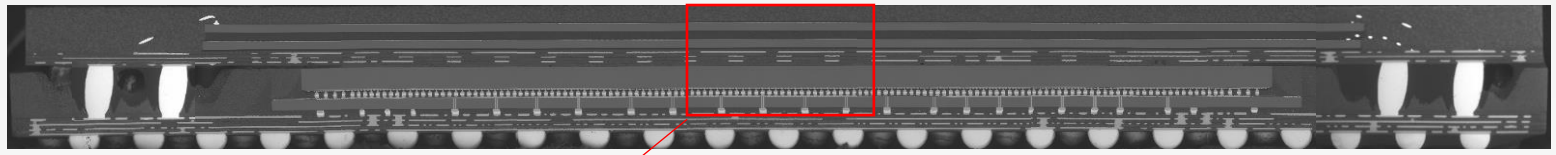
3D MCP Landscape

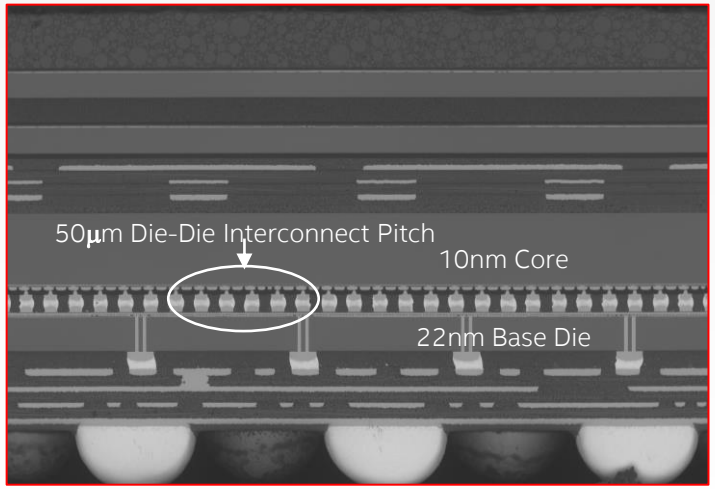


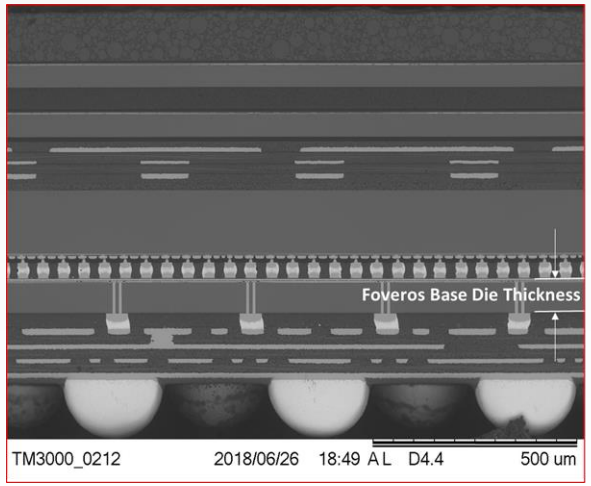


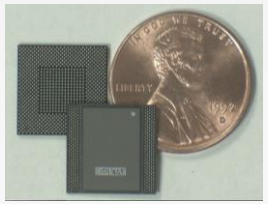
Transition from Solder Based Interconnects to Cu-Cu interconnects will be needed with shrinking bump pitch

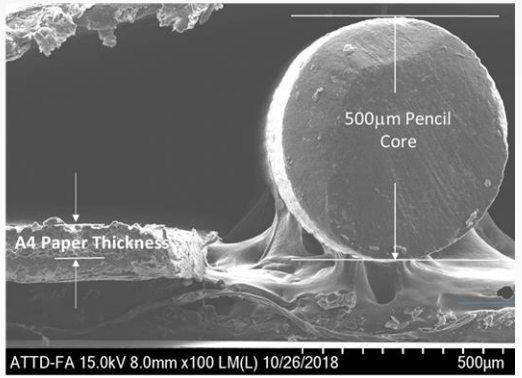
Intel Foveros : High Density 3D

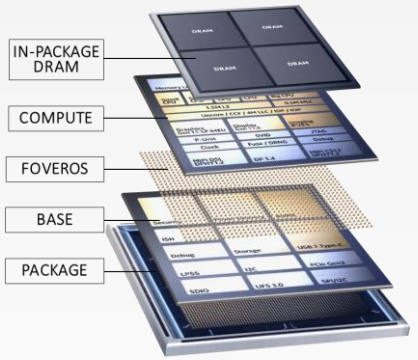


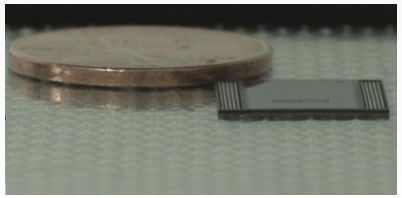












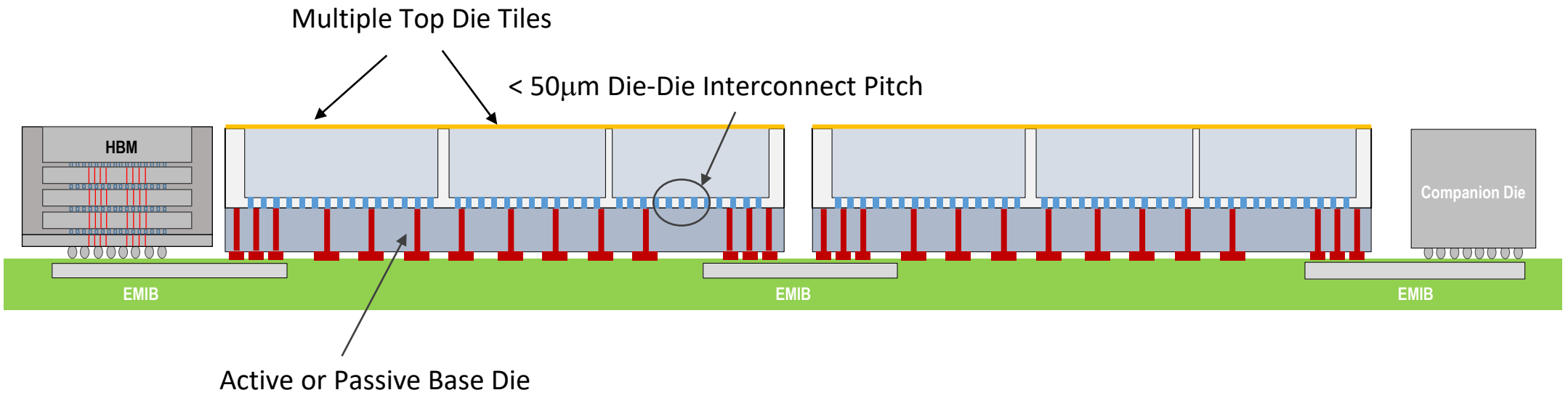
Compact Active Die Stacking : Initial Offering is Single Tile on Base die @ 50µm pitch

We are systematically Scaling tile count, Bump pitch

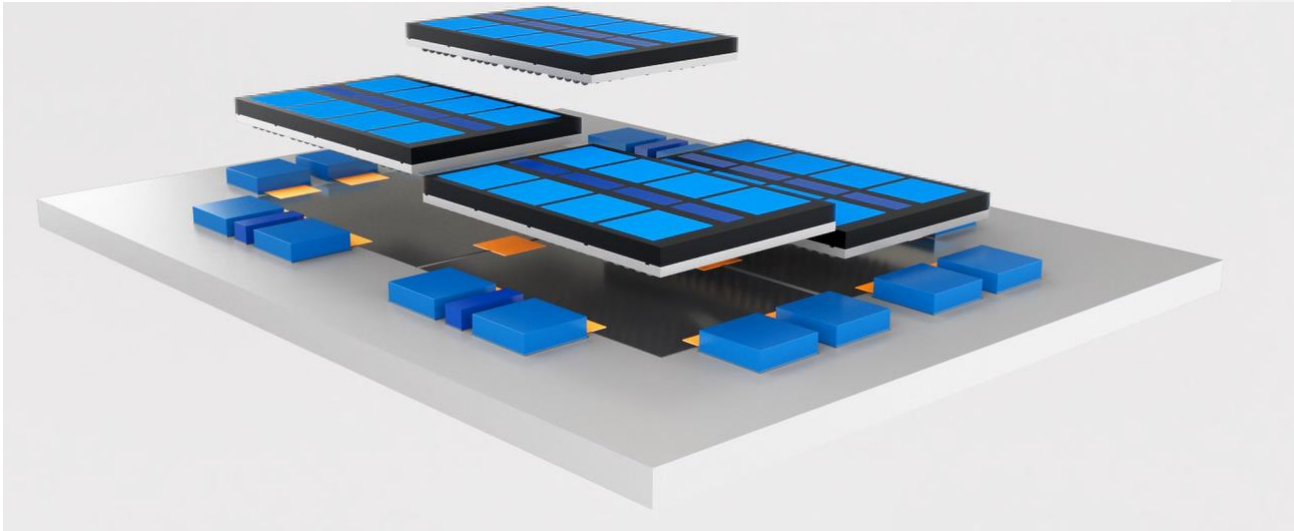
Meteor Lake @ 36µm Bump pitch

1. *D. Ingerly, et al. "Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices," 2019 IEDM*
2. *W. Gomes et al., "8.1 Lakefield and Mobility Compute: A 3D Stacked 10nm and 22FFL Hybrid Processor System in 12×12mm2, 1mm Package-on-Package," 2020 ISSCC*

Blending 2D and 3D



- Architecture enables >> reticle sized base die & High-Density Bridge links to companion Die
- Increased Partitioning Opportunities



Blending Planar and 3D MCPs (EMIB + Foveros)

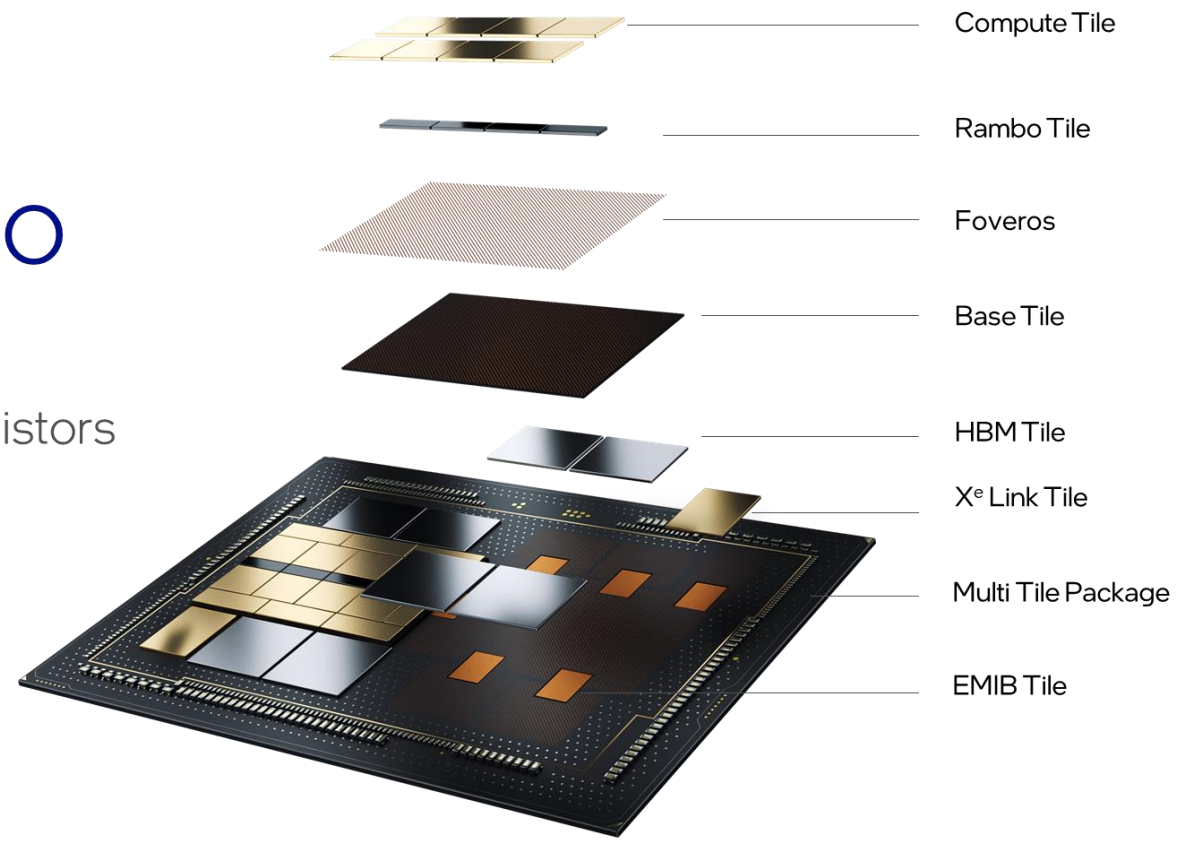
Ponte Vecchio

SOC

>100 Billion Transistors

47 Active Tiles

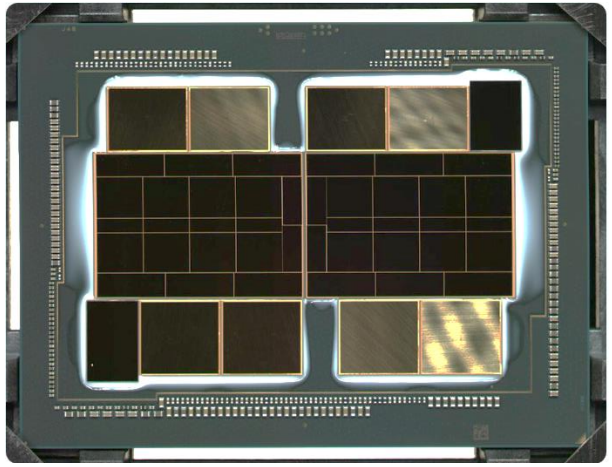
5 Process Nodes

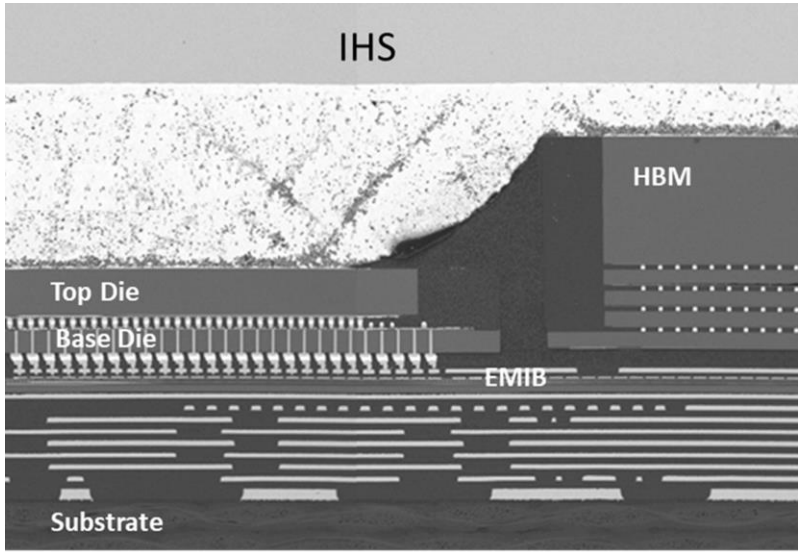


5

HI Enables Complex Integration → Exascale Computing

Ponte Vecchio



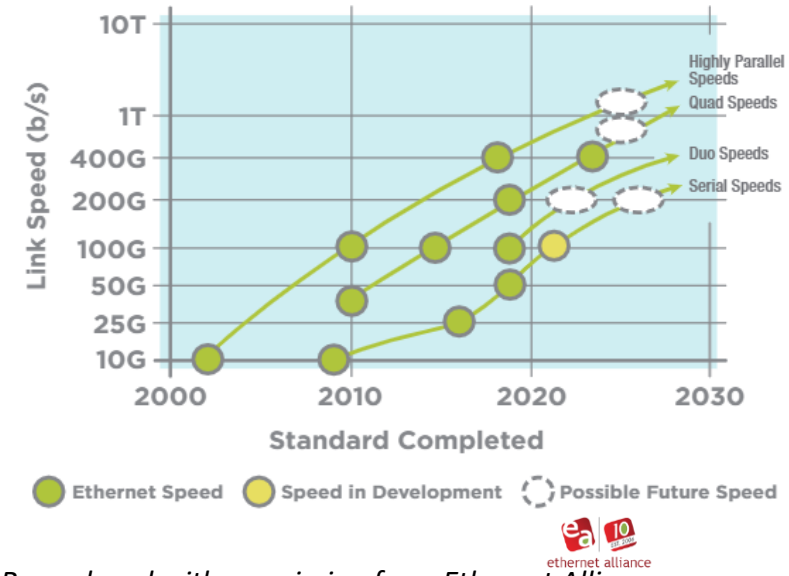


D2D Pitch	36um
Active Top Die Count Per Stack	16
Max Active Top Die Size	41mm^2
Base Die Size	650mm^2
EMIB Pitch	55um
Core Pitch (min)	100um
Memory (HBM)	8x
Package size	(77.5 x 62.5) mm
EMIB count	11

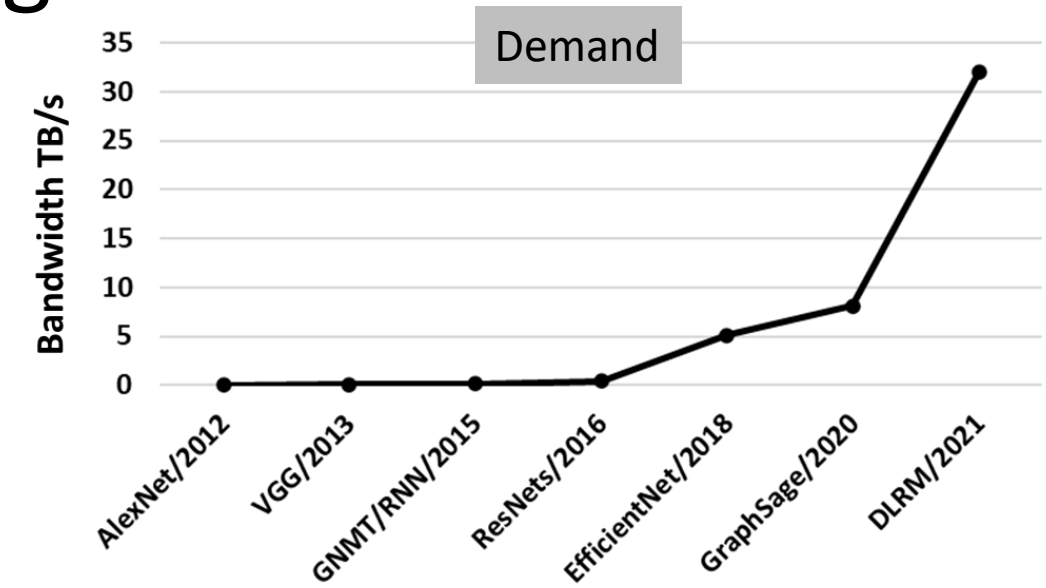
Intel implementing deep heterogeneous integration in product stack

Packaging Beyond Today

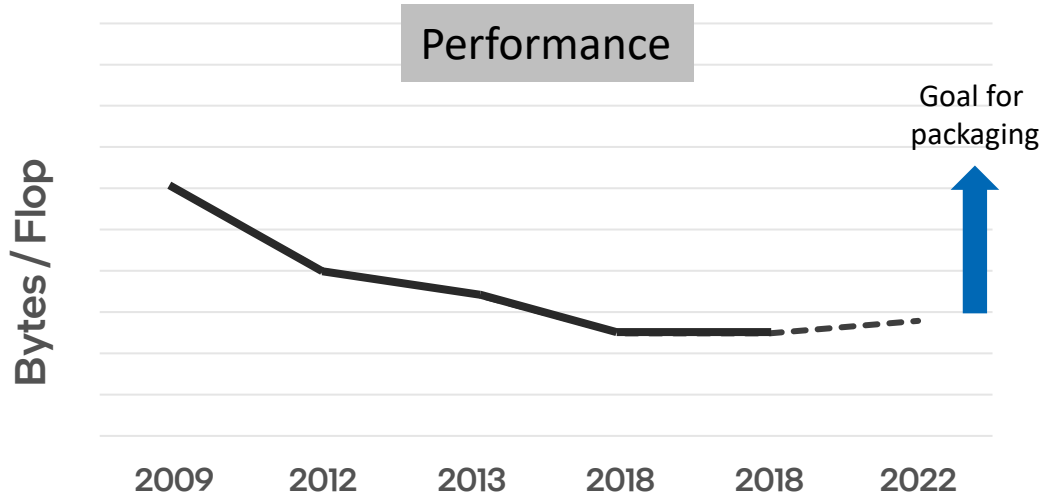
I/O Bandwidth & Speed Scaling Trends



Reproduced with permission from Ethernet Alliance



- Growing Network & Memory (BW + Speed) Demand
- As peak FLOPS grow BW will need to keep up
- BW Demand requires Continued Scaling of On-Package and Off-Package Interconnects



*2022 represents trends and not actual data

Interconnect Scaling to Enable Bandwidth Scaling

Generations		1	2	3	4	5
Raw Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	40	30	20	10
	IO/mm	500	667	1000	1500	2000
	IO/mm^2	331	625	1111	2500	10000
Signaling Speed (Gbps)		2	3	4	5.33	8

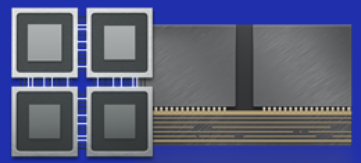
- Area Interconnects for 3D Architectures

Generations		1	2	3	4	5
Raw Bandwidth Density (Gbps/mm^2)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	40	30	20	15	10
	IO/mm^2	625	1111	2500	4444	10000
Signaling Speed (Gbps)		1.6	1.8	1.6	1.8	1.6

Source : Chapter 22 in IEEE Heterogeneous Integration Roadmap (https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2019-edition.html)

Continued leadership in Advanced Packaging

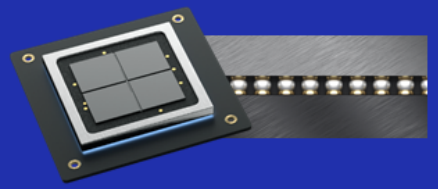
Embedded Multi-die Interconnect (EMIB)



bump pitch ≤ **55 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

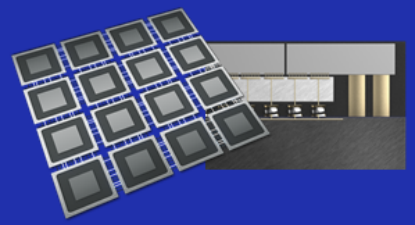
Foveros Technology



bump pitch **50-36 microns**

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

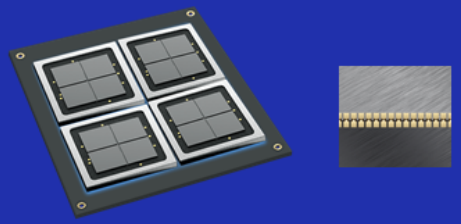
Foveros Omni



bump pitch **~25 microns**

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

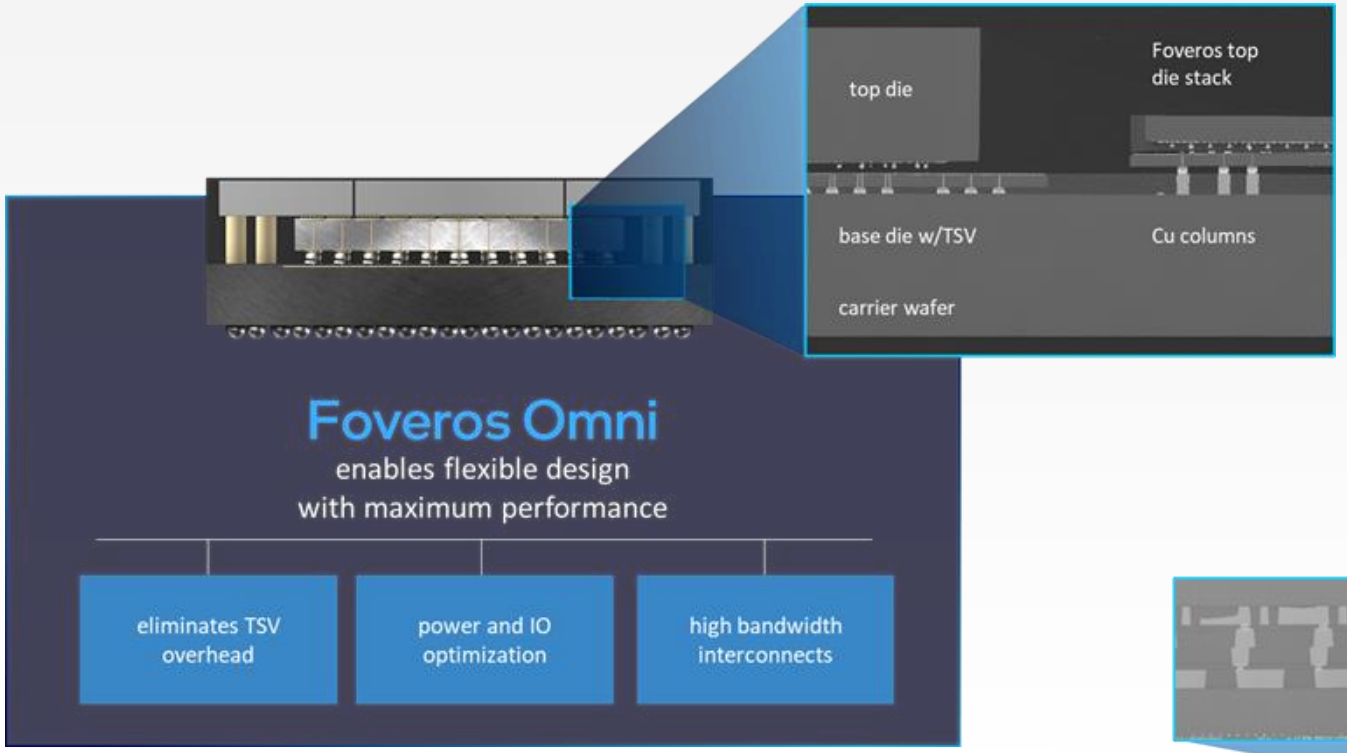
Foveros Direct



bump pitch **< 10 microns**

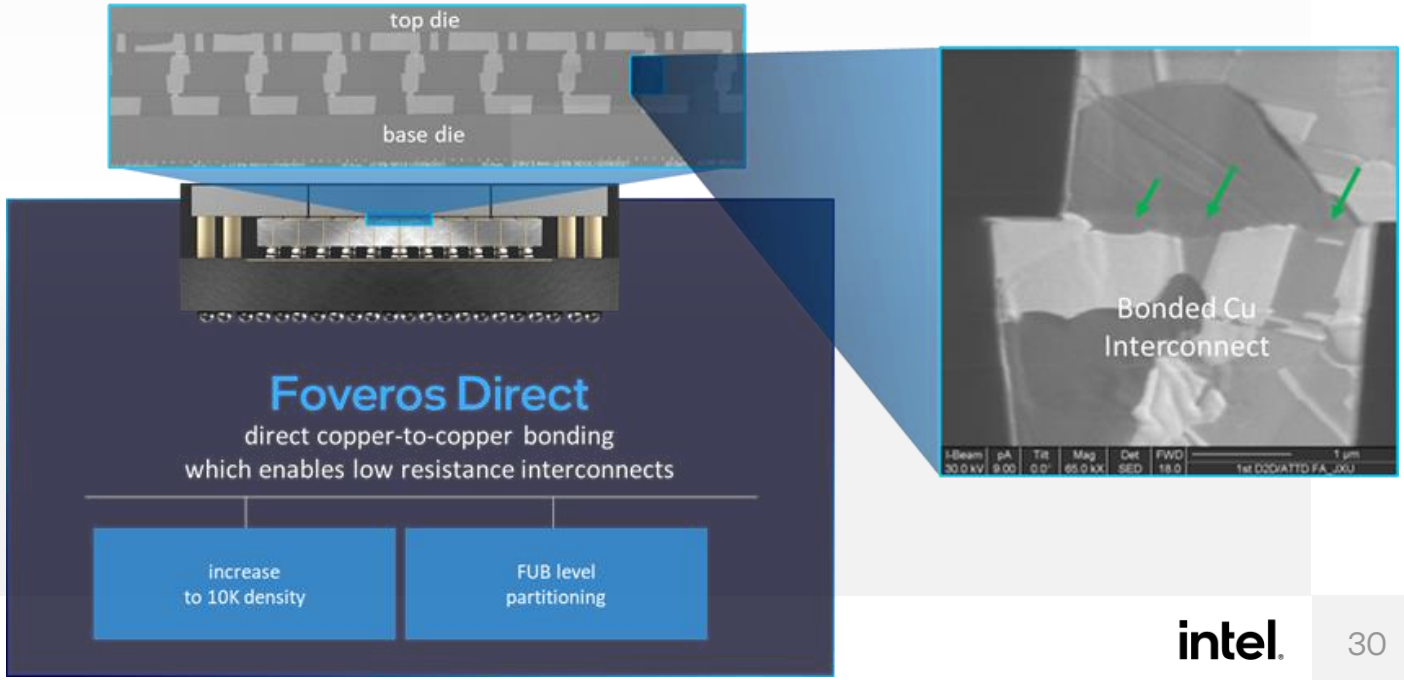
- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

Packaging Innovations: Foveros Omni and Foveros Direct



- Rich Interconnect Portfolio allows greater mix-and-match and better/independent interconnect optimization for Power and IO

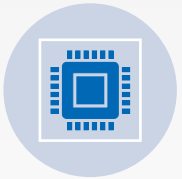
- Pitch Scaling from 25µm → ≤ 10µm leads to an order of magnitude increase in IO/mm^2 (1600 → ≥ 10,000)



What do we all need to work on?

The Package as a HI Platform – Key Focus Areas

Power-efficient, High Bandwidth On-Package IO links



Enable a diversity of off-package IO protocols

Deliver noise isolation for single ended and differential signals

Manage increasing cooling demands

Support complex power delivery architectures

Meet diverse application functionality ranging from high performance servers to flexible, wearable electronics

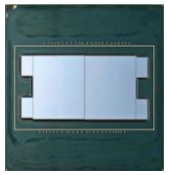
Meet a broad spectrum of reliability requirements for different market segments and applications

Provide cost effective, high precision quick turn assembly

Packaging has tremendous breadth : I will pick only a few areas for discussion today

intel

Heterogeneous Packaging: Materials & Mechanics Challenges and opportunities



Large Packages
- Large form factors
- Beyond reticle die complexes.
- Warpage management

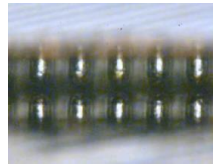
- Design & Assembly co-optimization
- Next Gen CUF & substrate materials

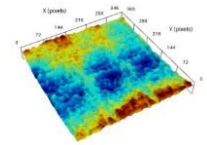
- Advanced flow& thermal simulation methods.
- Next Gen capillary underfills

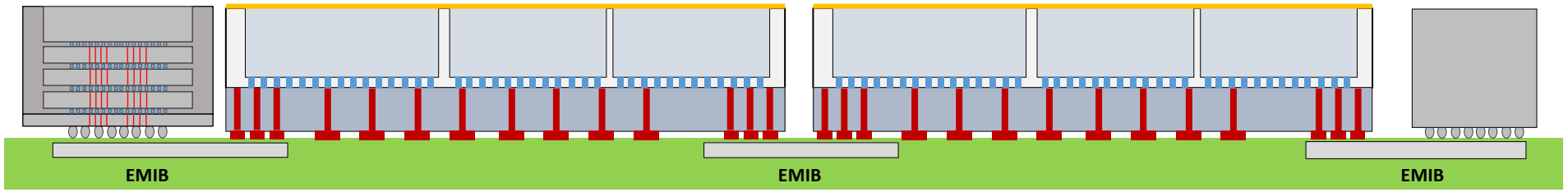
Better materials
- UF/mold: Flow, Warpage
- Fluxes: joint quality/cleanability
- Thermal interface materials

Fine pitch interconnect joint yield
- Die-Die, Die-Wafer, Die- Substrate
- Improved alignment/ bump Coplanarity
- Stacked die coplanarity

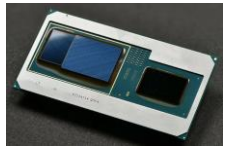
Advanced characterization& assembly methods







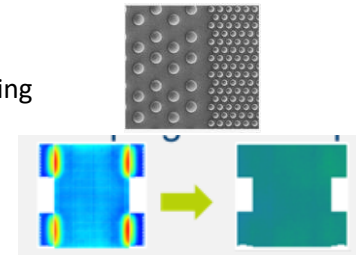
External IP/die/pkg integration
- Passivation/bump compatibility
- Design rule/ Design co-optimization.



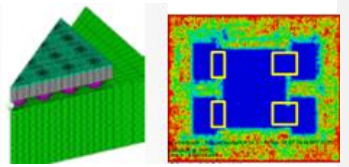
- Standardization of backend materials.

Advanced substrates
- Improved bump coplanarity
- Fine pitch/ Multi diameter bumping
- High density routing
- BU dielectrics & Organic core

- Design, manufacturing co-optimization.



Acceptable Reliability
- Materials for Temp-Cycle reliability
- Solder Joint reliability
- Electromigration
- Temperature/humidity/Bias

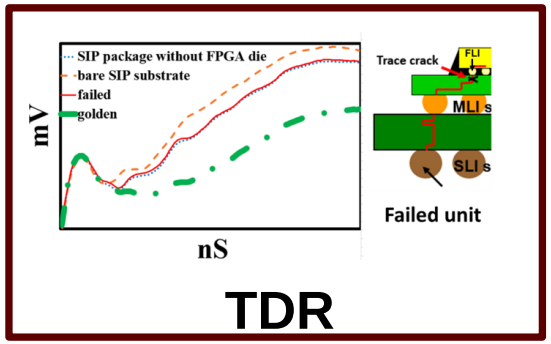


- Advanced Multiphysics simulation methods.
- Barrier metal innovation
- Material & solder advancements

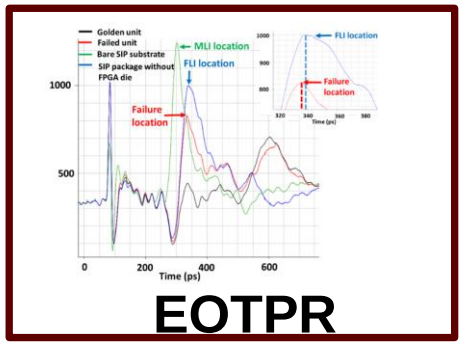
- Assembly and reliability challenges in Advanced Packaging present unique opportunities for material development , advanced simulation methods and metrologies
- Need Multiphysics based Co-optimization approaches and advanced metrologies to accelerate progress.

FI/FA Challenges: Fault isolation

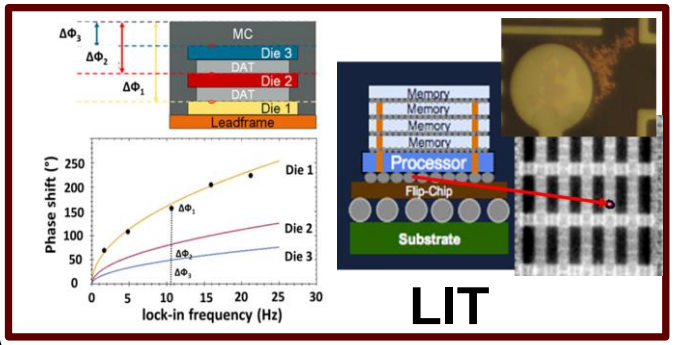
Typical fault isolation methods for electronic packaging



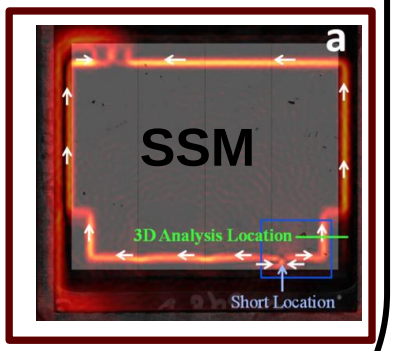
TDR



EOTPR



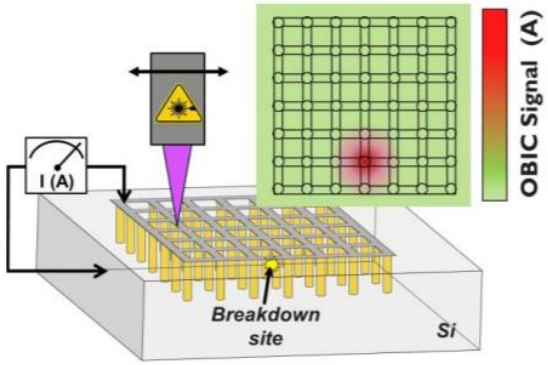
LIT

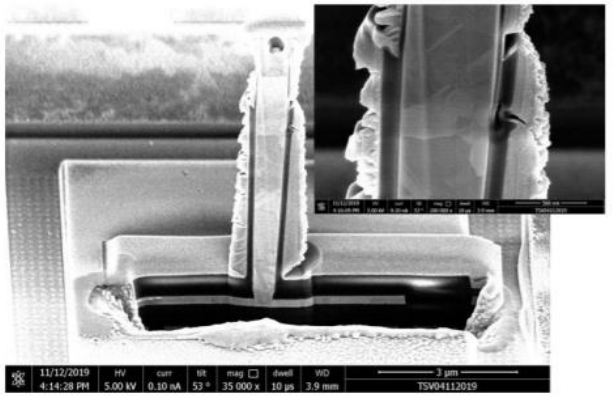


3D Microelectronic Packaging: From Architectures to Applications, 2nd edition, Springer, 2021, ISSN 1437-0387

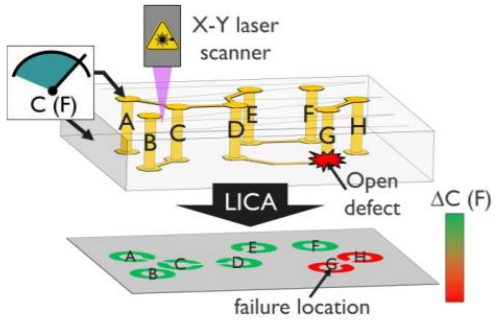
OBIC and LICA for 5µm pitch TSV breakdown and open

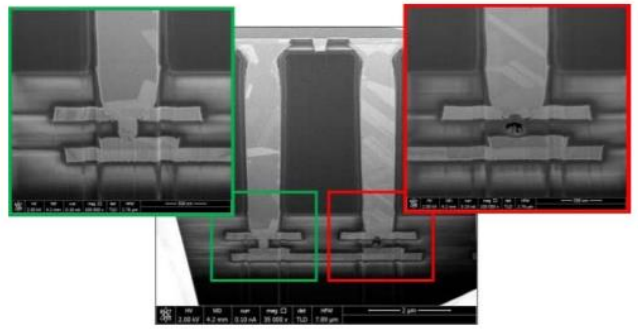
OBIC





LICA



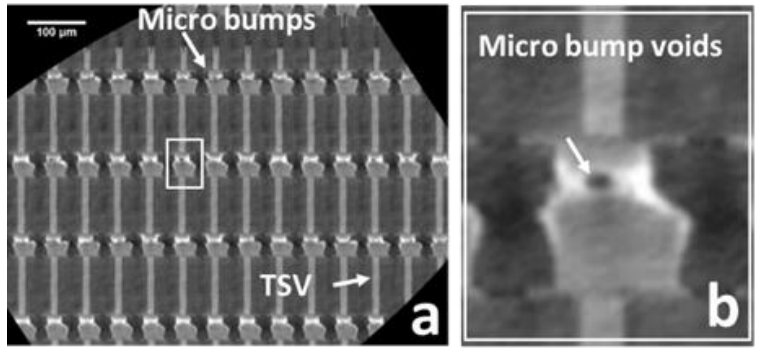


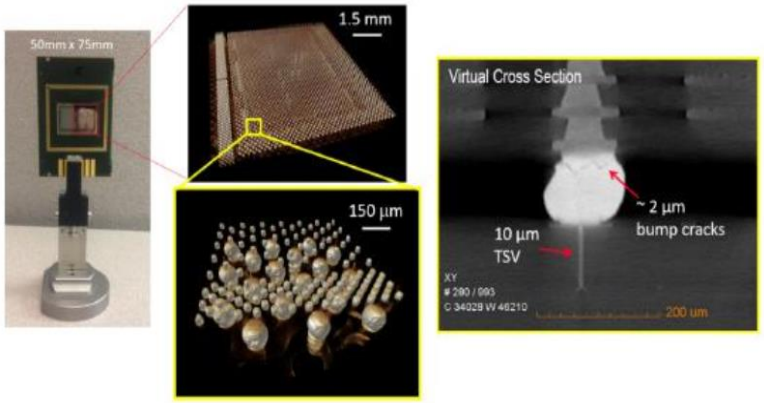
Kristof, Jacobs et al. IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY, VOL. 10, NO. 9, SEPTEMBER 2020

- Current capabilities will not suffice in future
- Will need Si FI/FA capabilities and/or develop hybrid capabilities

FI/FA Challenges: non-destructive imaging

Typical 3D X-ray for interconnect defects; no sample prep is needed





Cheryl Hartfield et. al. DOI: 10.1109/IPFA.2018.8452551

Nano 3D X-ray with <1µm resolution; Sample preparation is needed

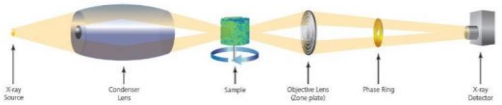
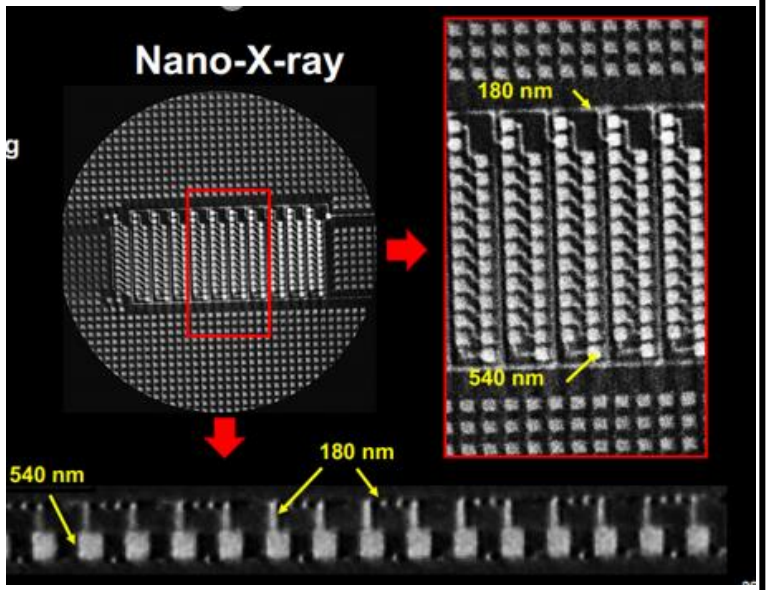


Figure 2. Schematic of X-ray architecture based on Fresnel-zone plate objectives [8].

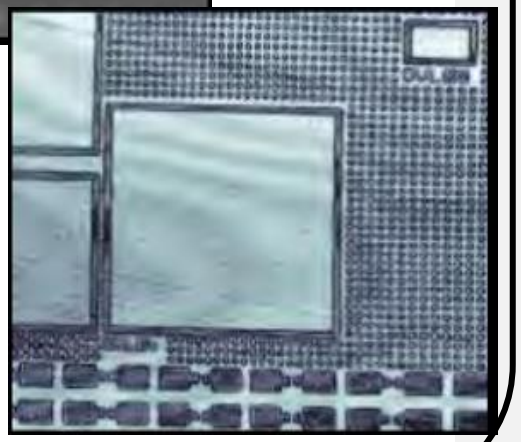


Christian Schmidt, et. al. ECTC 2018

CSAM resolution increases with frequency; need to thin down Si for GHz CSAM

775µm thick Si
100 MHz transducer
~50µm resolution

<5 um thick Si
1 GHz transducer
~1mµ ρεσolution

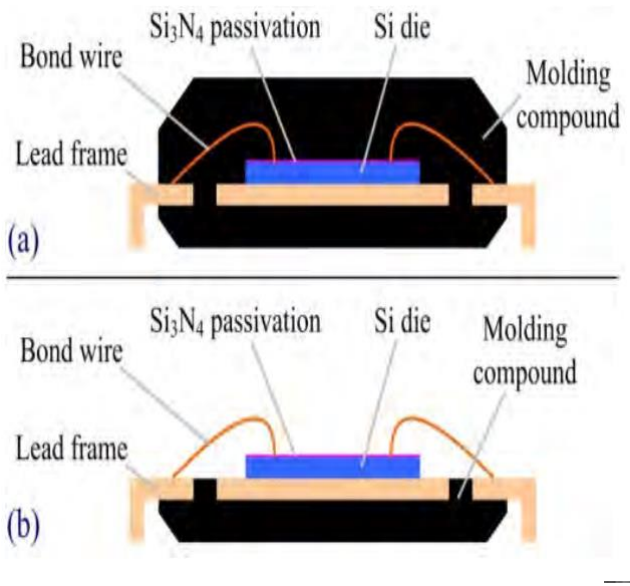


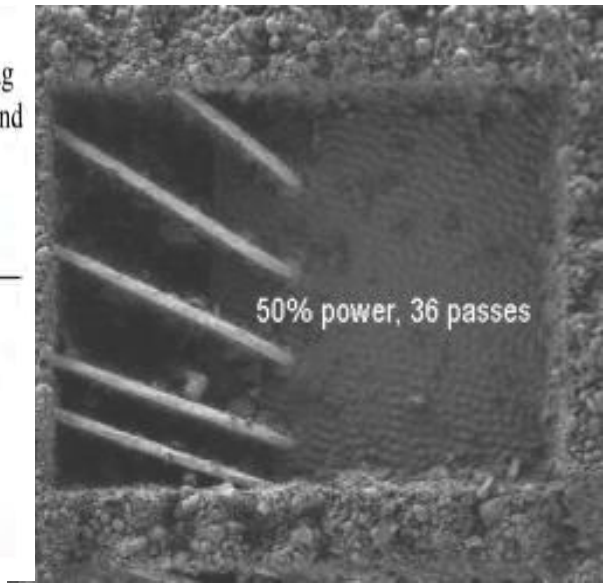
De Wolf et. al, ISTFA 2019

- Imaging subtle defects buried under multiple interfaces non-destructively is challenging
- Sample prep and long scanning time needed to reach high resolution for fine pitch TSV, HBI

FI/FA Challenges: sample preparation

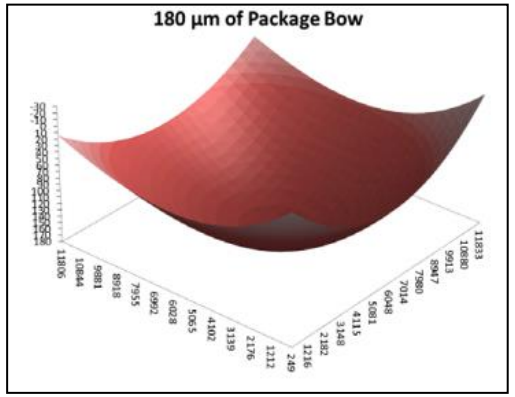
Athermal femtosecond laser decapsulation

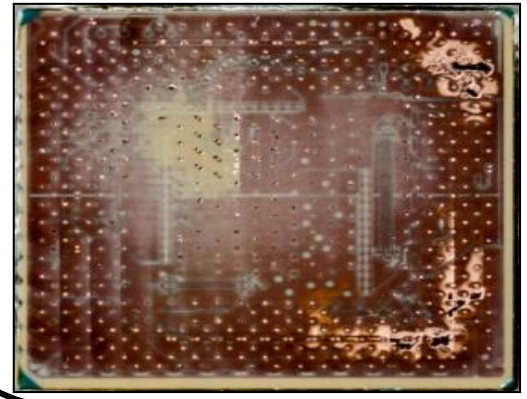


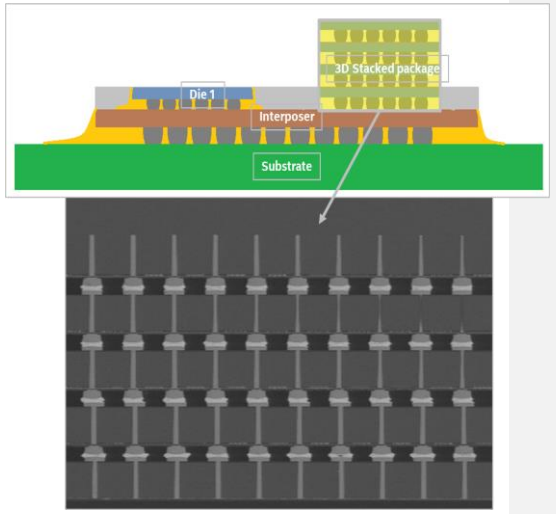


Edward Principe, ISTFA 2019 (adapted from the curtesy of Sina Shabazmohamadi at University of Connecticut)

Contour milling and ion milling

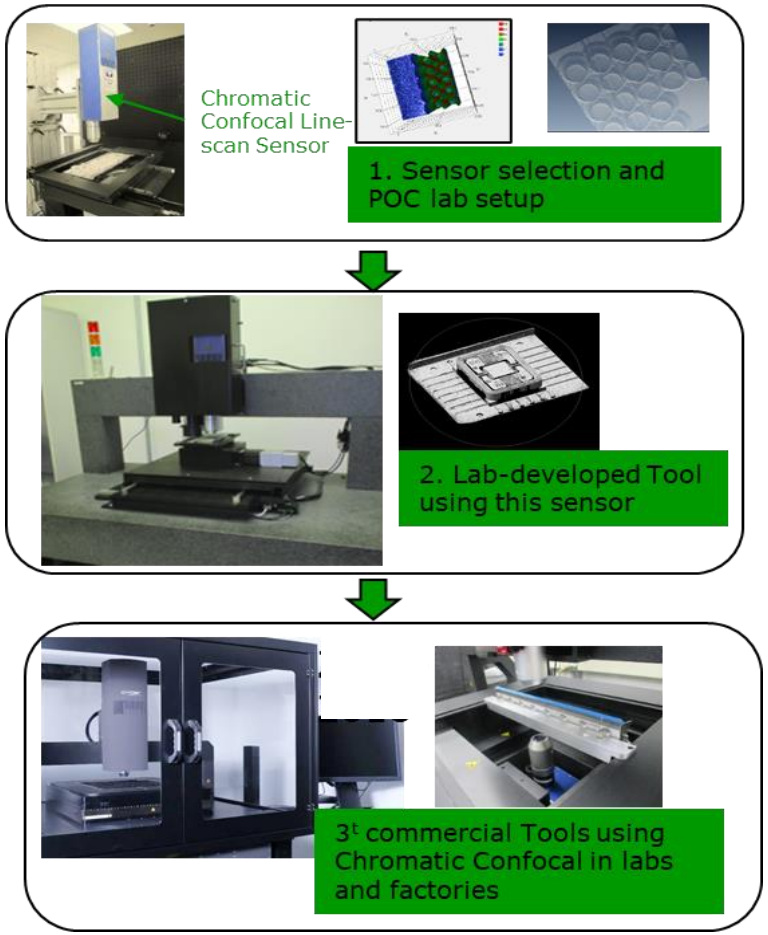




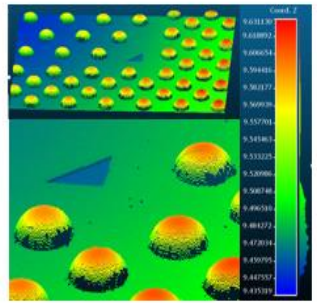


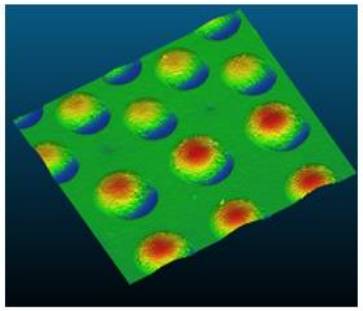
- Large area (deep and wide) artifact free cross-sectional exposure with high accuracy.
- Countering high and complex warpage shapes for uniform package delayering.
- Uniform Si thinning down for high resolution GHz CSAM, fault isolation and FIB cross-sections

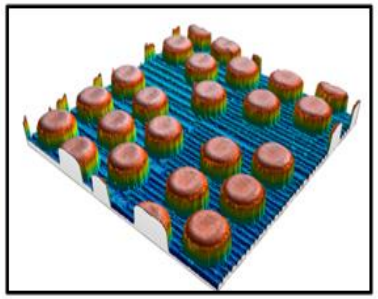
Dimensional Metrology Challenges: New Technology Adoption

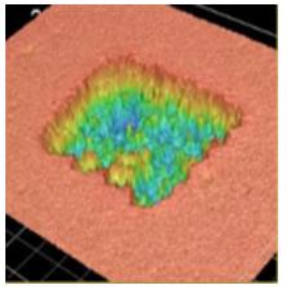


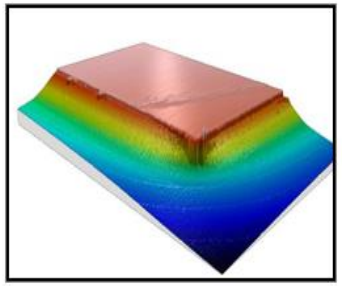
Intel drove metrology equipment companies to have early adoption of new technologies

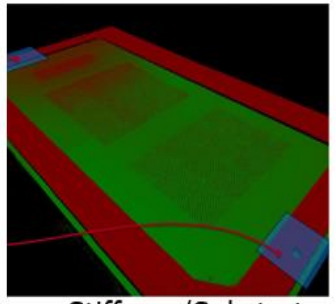

SLI Solder Balls

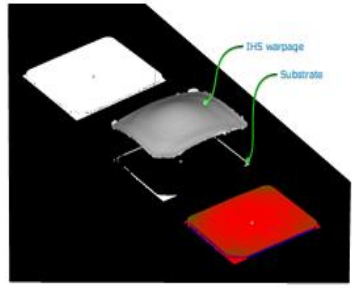

SLI Solder Paste


Wafer Bumps

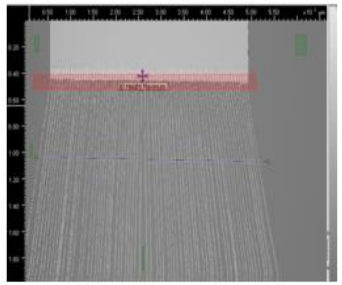

Laser mark


Epoxy Fillet Profile


Stiffener/Substrate



LID/Substrate Profile

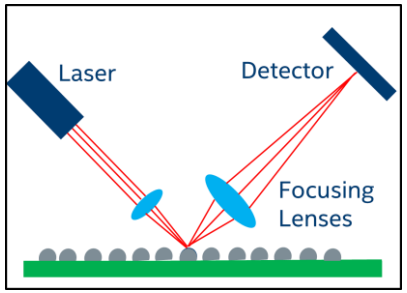

Wire Bond Profile

- How can we speed up new metrology technology development and adoption?

Metrology Challenges: Bump Height/Coplanarity

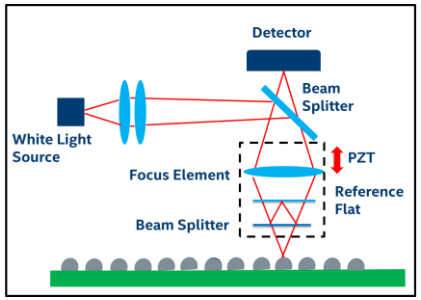
Typical bump metrologies for electronic packaging and their limitations:

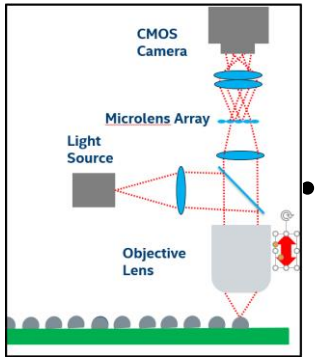
- **Triangulation**
  - **Accuracy**



- **Projection Moire'**
  - **Accuracy**

- **SWLI**
  - **Speed**

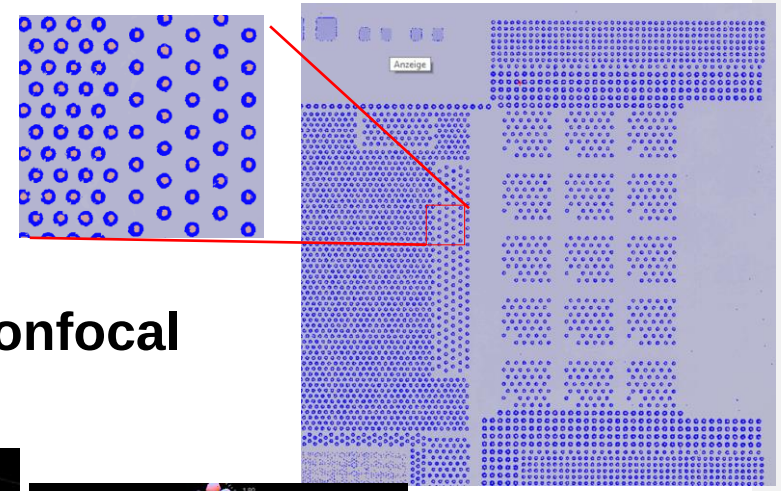




- **Confocal Microscopy**
  - **Speed**

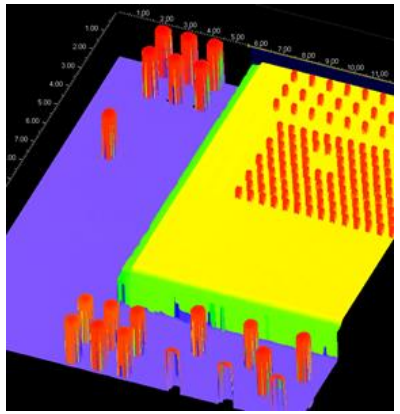
What's needed is a method with the accuracy of interferometry, and with sufficient vertical range without the time lost to vertical scanning.

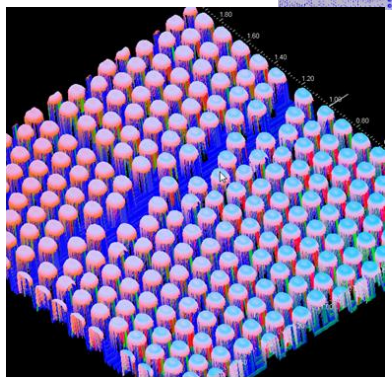
Possibilities:



- **Holography**

- **Chromatic Confocal Line Sensor**





Current methods are approaching their limits of accuracy, precision and speed as feature scaling continues and the number of features increases dramatically.

Summary

- Heterogeneous Integration (HI) is the vehicle for continued advances in Micro-electronics
- Advanced Packaging Architectures today provide unprecedented levels of Heterogeneous Integration in Client, Server and Discrete Graphics
- Future products face a slew of complex performance and manufacturing demands along multiple vectors
- We as a community must collaboratively extend advanced packaging technology envelopes along multiple vectors to meet the performance demands of the future
  - Engaging in Industry wide efforts to drive us forward e.g. (https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html)
  - FI/FA/MA/Metrology tool developments must keep pace with the Technology Roadmap
  - Packaging & Si BE are now indistinguishable – FA/FI metrologies including Si FI is critical

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Thank you